Analysis, Design, Simulation and Evaluation of Sigma-Delta (Σδ) Modulator for Gsm Synthesizer

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Abstract

The analysis, design, simulation and evaluation of 2nd, 3rd and 4th order ΣΔ modulator and loop filter respectively are discussed, in this paper, to show their impact on the performance of fractional-N PLL-FS for GSM system. All simulation results show that the system is stable. The resulting settling time, spurious level and phase noise at 20 MHz offset frequency of this synthesizer for 2nd, 3rd and 4th order ΣΔ modulator and loop filter respectively are 2.92 µs, -35 dBc, -164 dBc/Hz, 3.28 µs, -64 dBc, -186 dBc/Hz, 3.38 µs, -79 dBc and -190 dBc/Hz for 2nd, 3rd and 4th order respectively. These results show the improvement in the spurious level and phase noise by -19 dBc, -31 dBc/Hz for 3rd order system and -34 dBc, -35 dBc/Hz for 4th order system respectively compared to the published work. CppSim program and Matlab (R2007a) are used for the simulation of ΣΔ fractional-N PLL-FS.

Keywords: GSM, PLL, Loop filter, Sigma-Delta (ΣΔ), Frequency Synthesizer (FS).

Introduction

To constitute a complete transceiver for wireless communication systems, one indispensable building block, is required by both the receive and transmit path, is the Frequency Synthesizer (FS) to generate the frequency (or frequencies) signal. Wherever frequencies are translated, frequency synthesis is crucial to provide a clean, stable and programmable Local Oscillator (LO) signal. Programmable to address all frequency channels with fast switching and high resolution are required to perform the addressing sufficiently fast. The low noise level is vital for the quality and reliability of the information transfer [1].

Fractional-N Phase-Locked Loop (PLL)-FS technique is the most advanced and recent technique to satisfy these requirements. Fractional-N is a technique to achieve frequency resolution finer than the reference frequency. Fractional-N synthesis can be divided into two categories, classical fractional-N synthesis and sigma-delta (ΣΔ) fractional-N synthesis. The main performance limitation of the classical approach to fractional-N synthesis centers around the difficulty in creating a precise match between the noise cancellation Digital-to-Analog Converter (DAC) output and the phase error signal [2]. In ΣΔ fractional-N synthesis, the most popular technique used today to generate fractional divide values, and the spurious performance is improved through ΣΔ modulation of the divider control. The quantization noise introduced by dithering the divide value is therefore whitened and shaped to high frequencies, such that it is substantially filtered by the synthesizer dynamics [3].

GSM System

The GSM system is a system with a wide spread use and the typical configuration for GSM system is shown in Fig. (1). The main blocks for GSM system cell are Mobile Stations (MS) communicating with a network of Base Transceiver Station (BTS). Each cell in the cellular network requires a Radio Frequency (RF) carrier. The original cell is divided into three smaller cells. These cells share the same cell site but each has its own allocation of radio carriers. An RF carrier is a pair of radio frequencies. One is used in each direction (including transmission and reception) so that information may be passed in both directions simultaneously [4]. The frequency spectrum allocated for cellular system is only a narrow bandwidth. The bandwidth for the GSM system is 25 MHz. The transmitting and receiving frequencies in GSM are separated by 45MHz to avoid interference. The frequency bandwidth used for the downlink (from BTS to MS) is

(935-960) MHz. The frequency bandwidth for the uplink (from MS to BTS) is (890-915) MHz. The channel spacing is 200KHz [5]. Frequency synthesis is an essential technique employed in RF systems to achieve LO generation or direct modulation transmission. Radio Frequency (RF) system designers of Time Division Multiple Access (TDMA) based cellular systems, such as GSM, need LO or FS blocks capable of tuning to a new channel within a small fraction of each time slot. The suppression of reference spurs and phase noise is also critical for these modern digital standards. Base station and data transmission applications are now striving to utilize all the time slots available in each frame using a single synthesizer [6].

Frequency Synthesizer Parameters

Many different parameters must be considered to determine the cost, weight and power consumption of a synthesizer in a particular application. The most common parameters are described below [6, 7, 8]:

-Frequency resolution: This parameter is also referred to as the step size, and it specifies the minimum step size of the frequency increments.

-Settling time: This parameter is defined as the maximum amount of time required for the output frequency to reach a stable state at which the FS can hop from one frequency to another.

-Spurious signals: The spurious signal is defined as the ratio of the spur (also known as tone) power at a certain frequency offset to the carrier power expressed in dBc .

-Phase noise: It is the random fluctuations in the phase of output frequency of PLL [9]. The Single SideBand (SSB) phase noise is defined as the ratio of noise power in 1Hz bandwidth at a certain frequency offset (Δf) from the carrier (f_{out}) to the carrier power ($P_{carrier}$) expressed in dBc/Hz [8, 10]. A low phase noise VCO is an essential building block for the synthesizer. The phase noise requirements by the GSM 900MHz standard system are shown below in Table (1) [11].

System Layout

The general layout of the system design is shown in Fig. (2). The design parameters for the ΣΔ fractional-N PLL for GSM synthesizer are shown in Table (2).

Model of Quantization Noise for PFD/DAC

It is desirable to noise-shape the cancellation DAC's quantization noise. This is accomplished by processing the residue of the divider control with a ΣΔ modulator [12], as shown in Fig. (3). In order to achieve frequency resolution, the input word length of the ΣΔ modulator is chosen as 20-bits [13, 14]. The resolution of the ΣΔ modulator [15], is given by:

$$f_{resolution} = \frac{f_{ref}}{2^B} \quad (1)$$

where B: Number of bit input to the ΣΔ modulator.

f_{ref} : Reference frequency.

The output of the ΣΔ modulator (divider control), [16] is given by:

$$V(z) = F(z) + E_q \cdot (1 - z^{-1}) \quad (2)$$

where E_q: Quantization noise of the 1st order ΣΔ modulator.

$F(z)$: Input of the 1st order ΣΔ modulator.

B: Number of bit input to the ΣΔ modulator.

The design parameters of the 1st order ΣΔ modulator (divider control) are shown in Table (3 a). The quantization noise shaping transfer function for L^{th} order MASH ΣΔ modulator, [12] is given by:

$$NTF = (1 - Z^{-1})^L / \Delta \quad (3)$$

where Δ is the quantization step size.

The quantization noise reduction produced by the PFD/DAC is accomplished by dividing the noise transfer function of ΣΔ modulator by 2^B and is given by [12]:

$$NTF = \frac{(1 - Z^{-1})^L}{2^B} \quad (4)$$

where B : Number of bit of the DAC .

More levels are required to properly cancel the quantization noise [12]. The Signal-to-Quantization Noise Ratio (SQNR) achieved by a noise shaped PFD/DAC synthesizer, [17], is given by:

$$SQNR = 6.02 \times B + 1.76 \quad dB \qquad (5)$$

First-order Digital SD **Modulator (DAC Control) Design**

An accumulator may be considered a simple 1st order ΣΔ modulator as shown in Fig. (4). The 1-bit quantizer outputs is either 0 or 1 when it overflows [16, 18]. The output of the accumulator, at an arbitrary time is the sum of its input at that time and its contents one clock period earlier. If an overflow occurs, the full scale of the accumulator is subtracted. The output can thus be expressed as [19]:

$$\Sigma_n = x_i + \Sigma_{n-1} - y_i \qquad (6)$$

$$y_i = x_i + (\Sigma_{i-1} - \Sigma_i) \qquad (7)$$

$$y_i = x_i \quad (\Sigma_i \quad \Sigma_{i-1}) \qquad (8)$$

The *z*-transformation of eq. (8) is :

$$Y(z) = X(z) - \Sigma(z) \cdot (1 - z^{-1}) \qquad (9)$$

The z-transformation of 1st order ΣΔ modulator is:

$$Y(z) = z^{-1} \cdot X(z) + (1 - z^{-1}) \cdot E(z) \qquad (10)$$

Comparing eq. (9) with eq. (10) shows the similarity between them. Ignoring the latency of one clock period in the signal path of the ΣΔ modulator, and treating the contents of the digital accumulator as the negative of the quantization error, the equations are identical. The design parameters of the 1st order ΣΔ modulator (DAC control) are shown in Table (3 b).

Second-order Digital SD **MASH Modulator (DAC Control) Design**

A second order modulator is constructed by cascading two first-order modulators as shown in Fig. (5). The input is fed to the first stage and the negative of the quantization error from the first stage is used as the input to the second stage. Finally, the outputs of the stage are combined together to form a final output after passing through the error cancellation network, which removes the quantization error components from all the stages except the last one [20]. The output of the second-order MASH modulator is given by eq. (11) [21]. The design parameters of the 2nd order ΣΔ modulator (DAC control) are shown in Table (4).

$$Y(z) = F(z) + (1 - z^{-1})^2 \cdot Eq_1(z) \qquad (11)$$

Third-order Digital SD **MASH Modulator (DAC Control) Design**

A third-order modulator is constructed by cascading three first-order modulators as shown in Fig. (6). The input is fed to the first modulator and the negative of the quantization error from the first and second modulator is used as the input to the second modulator and third modulator, respectively. Finally, the outputs of each modulator are combined together to form a final output after passing through the error cancellation network, which removes the quantization error components from all the modulators except the last one [16, 18]. The output of the third-order MASH modulator is given by eq. (12) [21]. The design parameters of the 3rd order ΣΔ modulator (DAC control) are shown in Table (5).

$$Y(z) = F(z) + (1 - z^{-1})^3 \cdot Eq_2(z) \qquad (12)$$

Simulation and Results

The C++ language offers the flexibility of computing system behavior in any manner desired. CppSim works in conjunction with Sue2 [22]. CppSim uses Sue2 as its schematic editor for entering designs. Simulations are run through either CppSim or Matlab. The simulation approach taken with CppSim simulator is to represent the various blocks in a system as objects that update their outputs one sample at a time based on inputs that specify one sample at a time. The influences of the inputs on the outputs of each block are determined by their specified behavior, which is set at the beginning of a simulation run. The block behavior can be a function of state information as well as the block inputs. The state information is preserved inside its

respective block so that the overall simulator does not need to keep tracking it [22]. All blocks of ΣΔ fractional-N PLL synthesizer simulations were done using the CppSim program shown in Fig. (7).

PLL Output Spectrum Simulation

A 26 MHz reference frequency is used to generate an output frequency of 900 MHz. A closed loop bandwidth of 1 MHz is desired with type II PLL. The VCO noise is entered as -190 dBc/Hz at 20 MHz offset from the carrier. Phase detector noise, which represents the sum of charge-pump noise, reference jitter and divider jitter is set to -110 dBc/Hz. The VCO phase noise required for GSM synthesizer is -162 dBc/Hz at 20 MHz offset frequency, as shown in Table (1). VCO phase noise to reach -190 dBc/Hz at 20 MHz offset frequency is the goal of this paper. In the first simulation of the system, it is assumed that the quantization step size, Δ, of MASH ΣΔ modulator is 1 to show the impact of ΣΔ quantization noise. The simulations for 2^{nd}, 3^{rd} and 4^{th} order ΣΔ modulator are shown in Figs. (8), (9) and (10) respectively. The simulations show that the GSM phase noise, $\mathcal{L}(f)$, specifications are not met in the above design due to the ΣΔ quantization noise which dominates a wide frequency range.

Improvement of phase noise performance for synthesizer

The overall phase noise performance of the synthesizer, SSB, for 2^{nd} , 3^{rd} and 4^{th} order ΣΔ modulator is shown in Figs. (11 a), (12 a) and (13 a) respectively. The differences between these simulation results are shown in Table (6). The output spectrum of PFD/DAC PLL synthesizer for 2^{nd}, 3^{rd} and 4^{th} order ΣΔ modulator is shown in Figs. (11 b), (12 b) and (13 b) respectively.

Discussion of Simulation Results

1. The quantization noise of ΣΔ modulator is reduced by a factor of 2^B, where B is the number of bits in the PFD/DAC, so that the quantization noise of ΣΔ modulator becomes below the VCO noise and detector noise.
2. Increasing the order of ΣΔ modulator improves the spurious performance. The quantization noise of the modulator is pushed to high frequencies. To suppress this noise, the loop filter roll off must be at least the same.
3. Mismatch between the unit elements of the PFD/DAC is solved by DWA technique. DWA proves its ability to convert fractional spur noise into a broadband, shaped noise that appears to have the same profile as the quantization noise spectrum.
4. Time mismatch between the two phase paths that generates the charge box is processed by phase swapping. It was found that phase swap improves the spurious performance by converting the spurious energy into a broadband noise source.
5. Sample and hold circuit has improved the performance of the system by eliminating the residual fractional spurs as well as the spur at the reference frequency that occurs due to the mismatch shaping of the PFD/DAC output.

Conclusions

The ΣΔ fractional-N PLL-FS is designed to generate a frequency signal according to GSM system standard specifications. The simulation results show that the increasing order of the ΣΔ modulator from 2^{nd} order to 4^{th} order improves the phase noise performance of FS by -186 dBc/Hz for 3^{rd} order and -190 dBc/Hz for 4^{th} order if compared with 2^{nd} order. The minimum numbers of bits required to reduce the effect of quantization noise to the level below the VCO noise are found 14, 13 and 12 bit for 2^{nd}, 3^{rd} and 4^{th} order ΣΔ modulator respectively. The closed loop bandwidth of PLL is chosen to be 1 MHz to improve the settling time of FS. The settling time results of 2^{nd}, 3^{rd} and 4^{th} order system are 2.92 μs, 3.28 μs and 3.38 μs respectively.

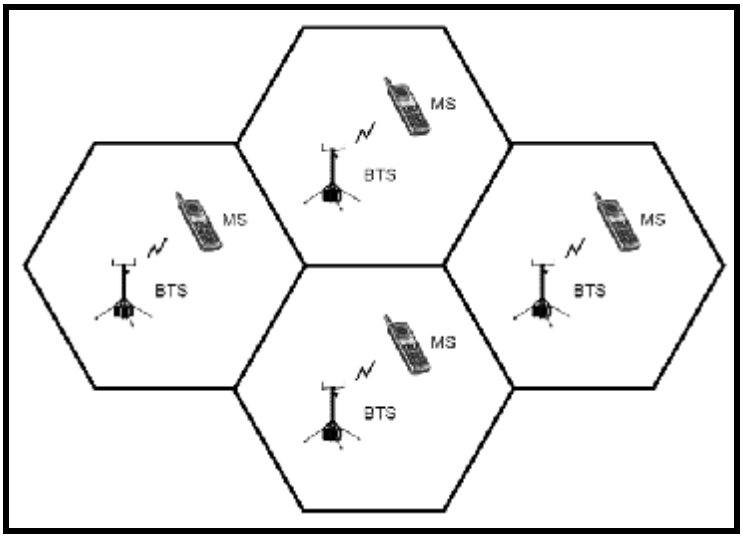

Fig. (1) Cellular system.

Table (1)
Phase noise specifications for GSM 900MHz standard system.

Offset frequency (MHz)	*Phase noise requirement (dBc/Hz)*
3.0	-123
6.0	-129
10	-150

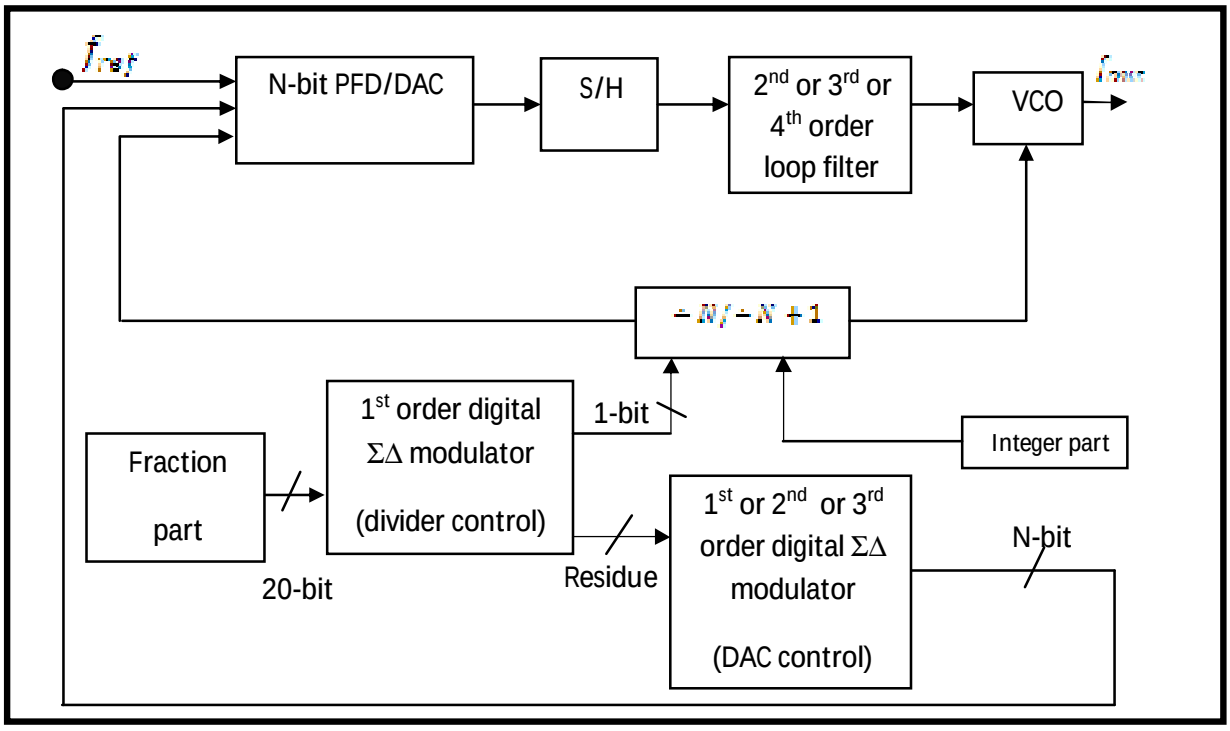

Fig. (2) Block diagram of system.

Table (2)
Design parameters.

Parameter	*Proposed system parameters*
Output frequency	900 MHz
Reference frequency	26 MHz [5]
Loop bandwidth	1 MHz, To improve settling time
Charge pump current	5mA
Filter (Order, Type)	2^{nd}, 3^{rd} and 4^{th} order, passive type
ΣΔ modulator (Order, Type)	2^{nd}, 3^{rd} and 4^{th} order, MASH type
Divider value	34.6154
PFD/DAC resolution	14-bit (2^{nd} order), 13-bit (3^{rd} order) and 12-bit (4^{th} order)
PFD noise	-110 dBc/Hz

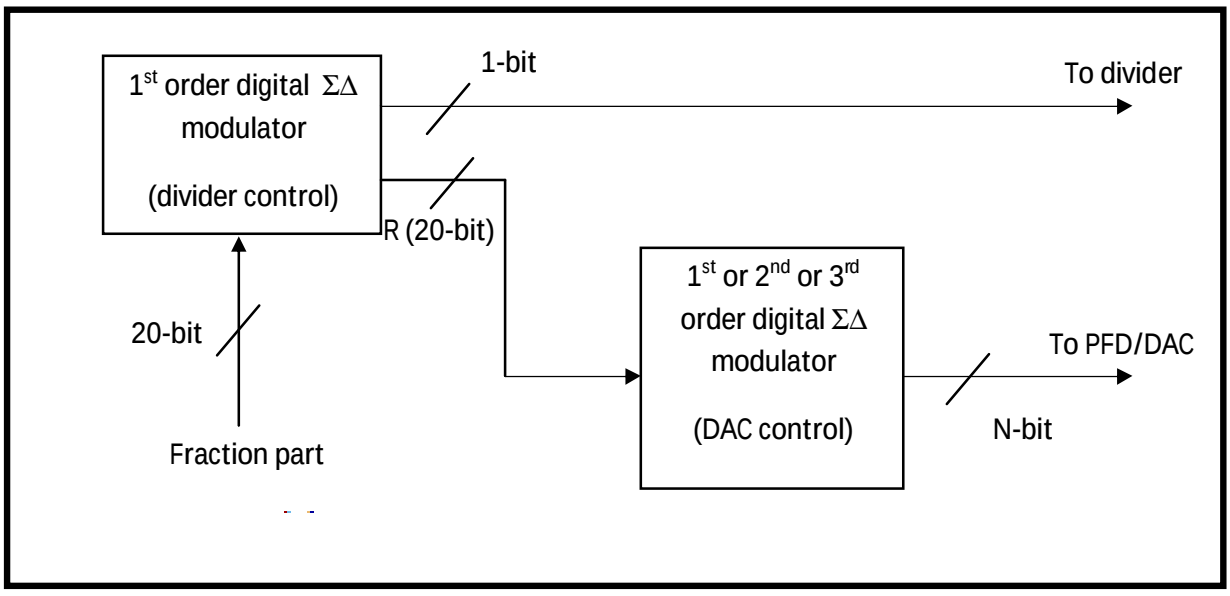

Fig. (3) Model of noise shaped in PFD/DAC.

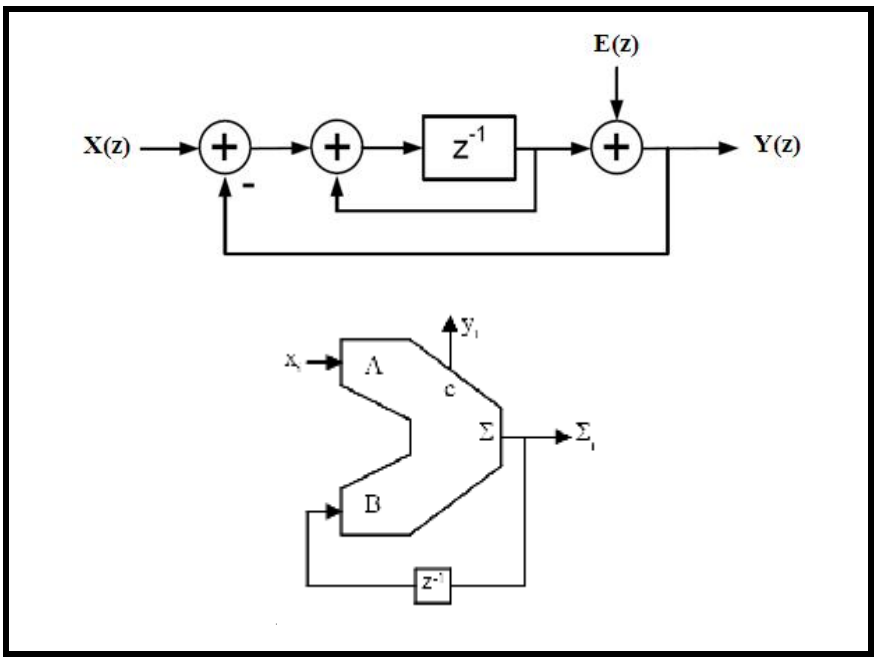

Fig. (4) Similarity of the SD modulator and the accumulator.

Table (3 a)
1st order SD modulator (divider control) parameters.

Parameters	***Value***
Input bit	20-bits
Output bit	1-bits
Fractional resolution	25 Hz
Sampling frequency	26 MHz

Table (3 b)
1st order SD modulator (DAC control) parameters.

Parameters	***Value***
Input bit	20-bits
Output bit	14-bits
Fractional resolution	25 Hz
Sampling frequency	26 MHz

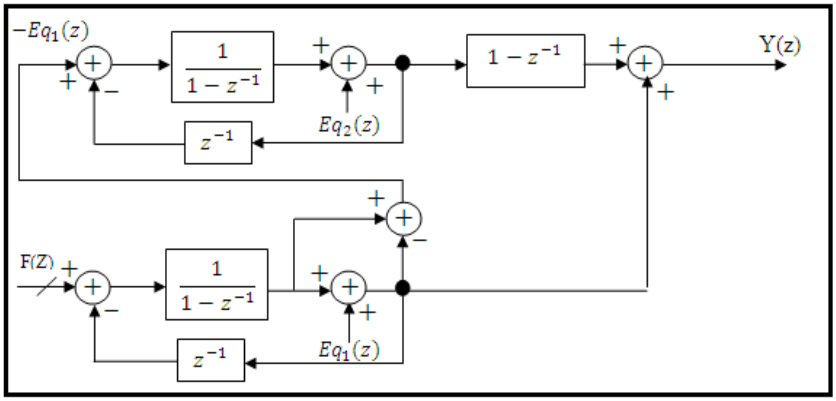

Fig. (5) Second-order MASH 1-1 SD modulator.

Table (4)
2nd order SD modulator parameters.

Parameters	*Value*
Input bit	20-bits
Output bit	13-bits
Fractional resolution	25 Hz
Sampling frequency	26 MHz

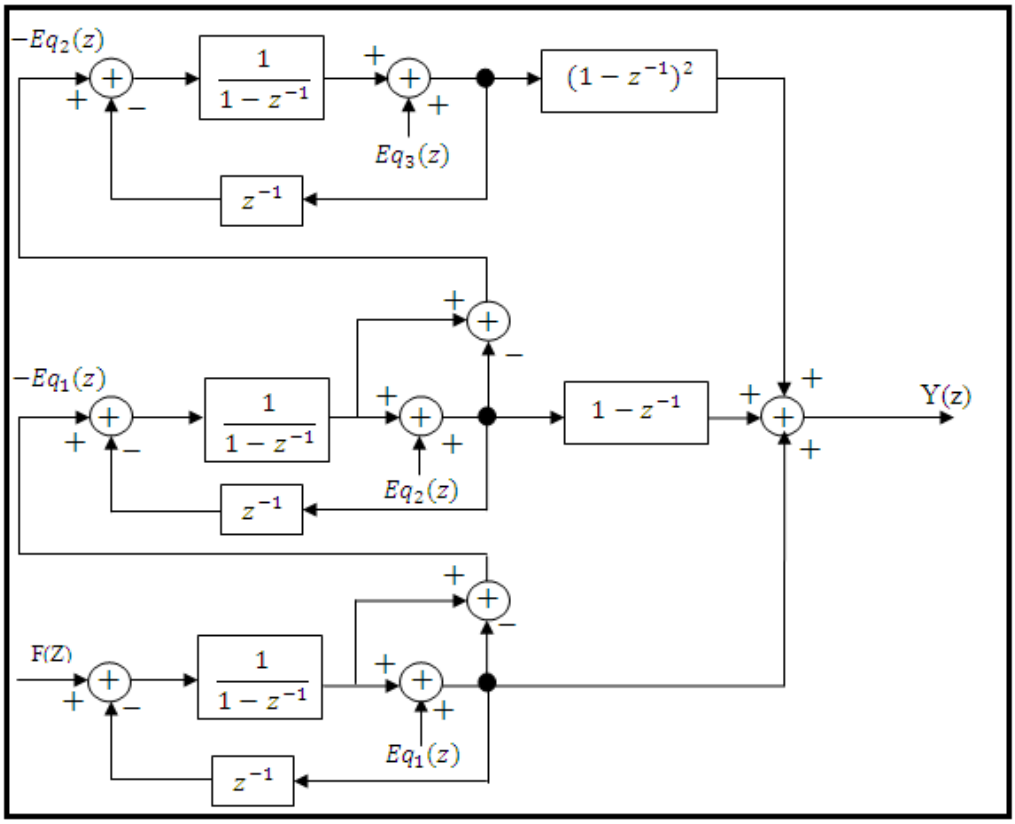

Fig. (6) Third-order MASH 1-1-1 SD modulator.

Table (5)
3rd order SD modulator parameters.

Parameters	*Value*
Input bit	20-bits
Output bit	12-bits
Fractional resolution	25 Hz
Sampling frequency	26 MHz

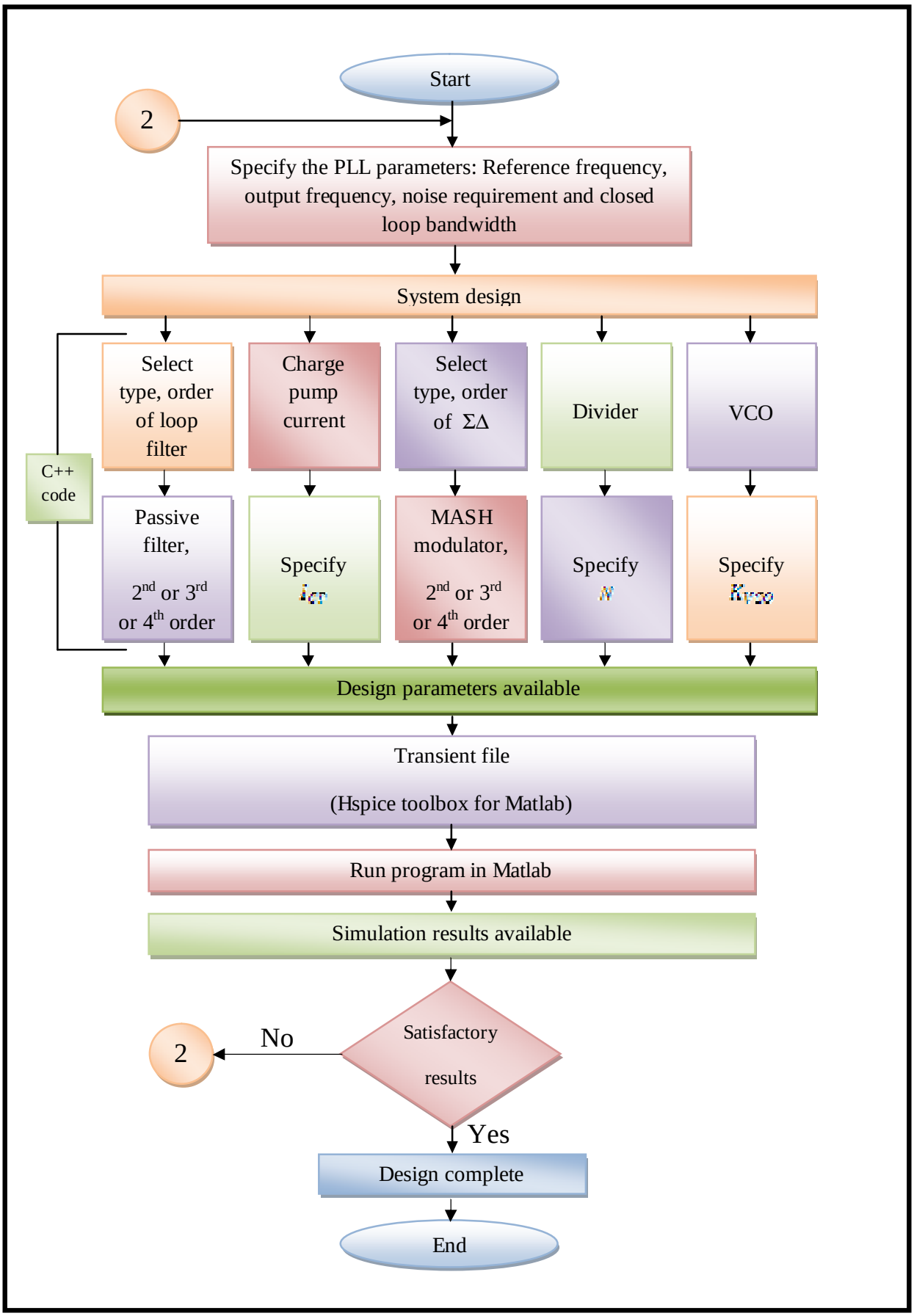

Fig. (7) Flow chart of the SD fractional-N PLL simulation program.

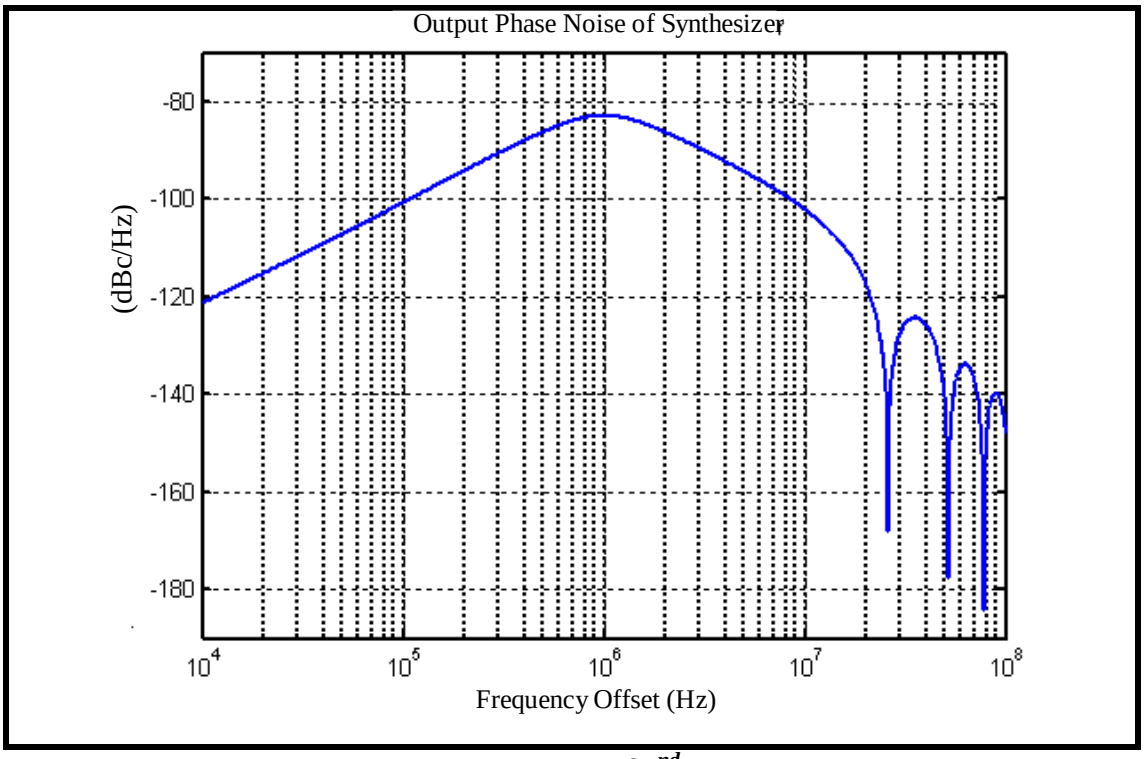

Fig. (8) Simulation showing the impact of 2nd order SD quantization noise.

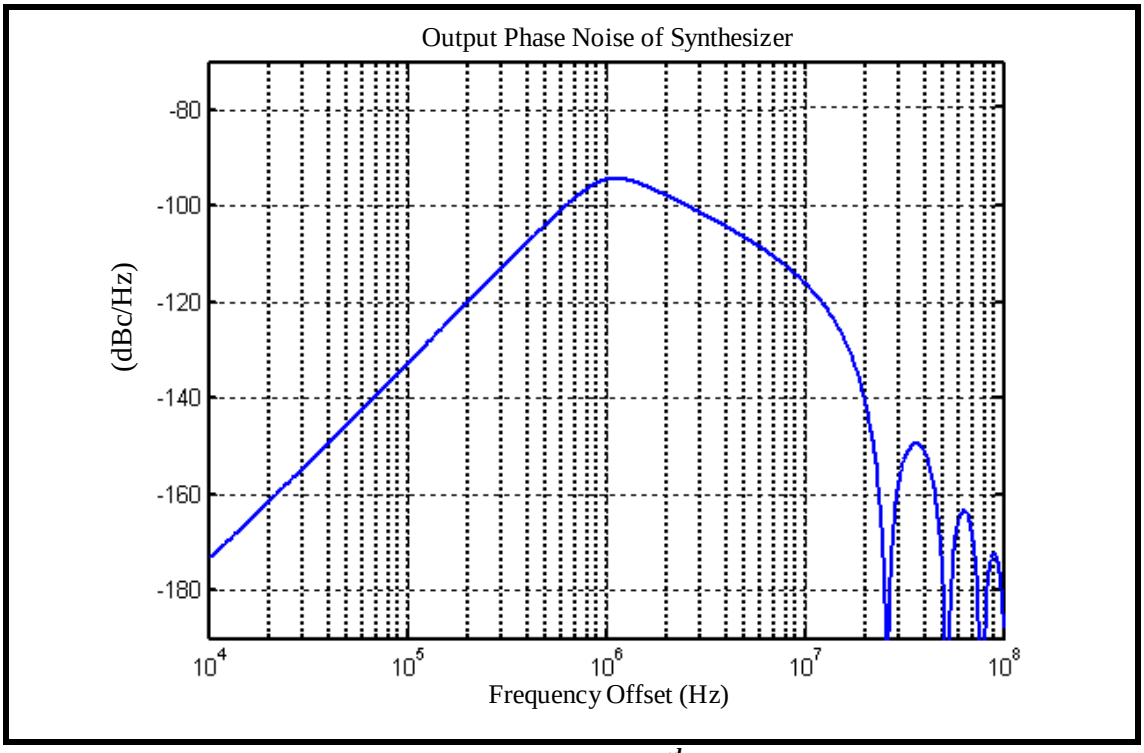

Fig. (9) Simulation showing the impact of 3rd order SD quantization noise.

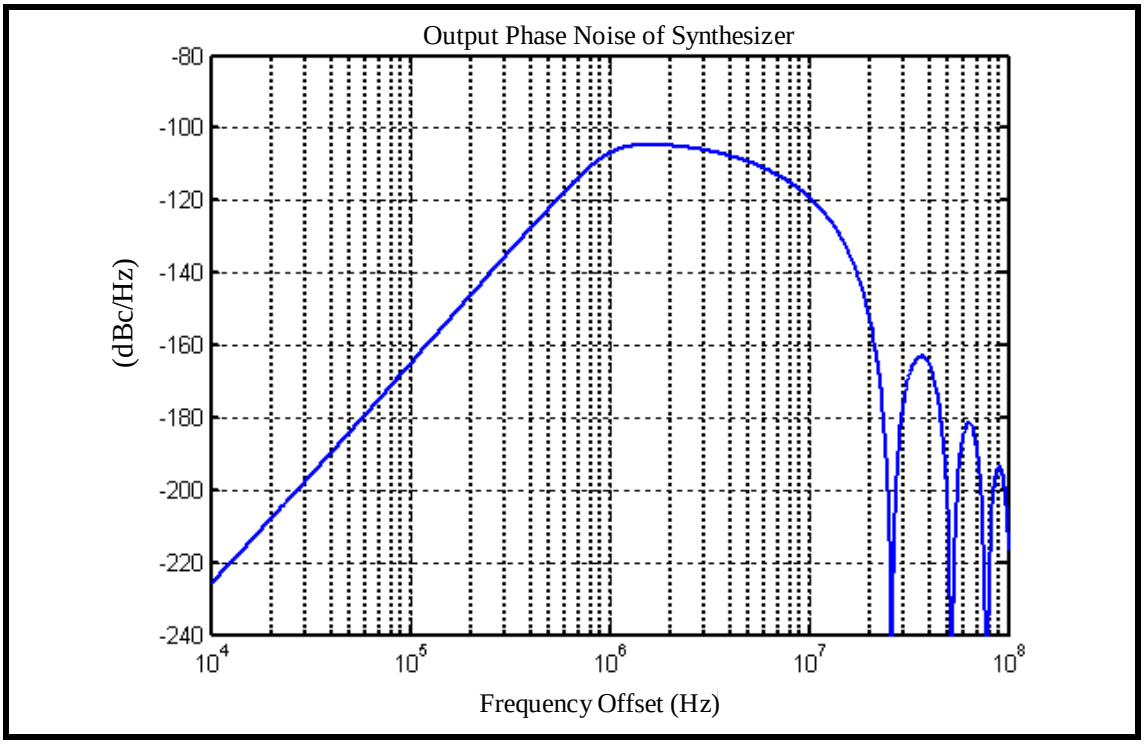

Fig. (10) Simulation showing the impact of 4th order SD quantization noise.

Table (6)
Phase noise simulation results.

Offset frequency	*Phase noise requirement (dBc/Hz)*	*Phase noise result for 2nd order system (dBc/Hz)*	*Phase noise result for 3rd order system (dBc/Hz)*	*Phase noise result for 4th order system (dBc/Hz)*
3.0 MHz	−123	−134	−141	−142
6.0 MHz	−129	−144	−159	−162
10 MHz	−150	−154	−171	−180
20 MHz	−162	−164	−186	−190

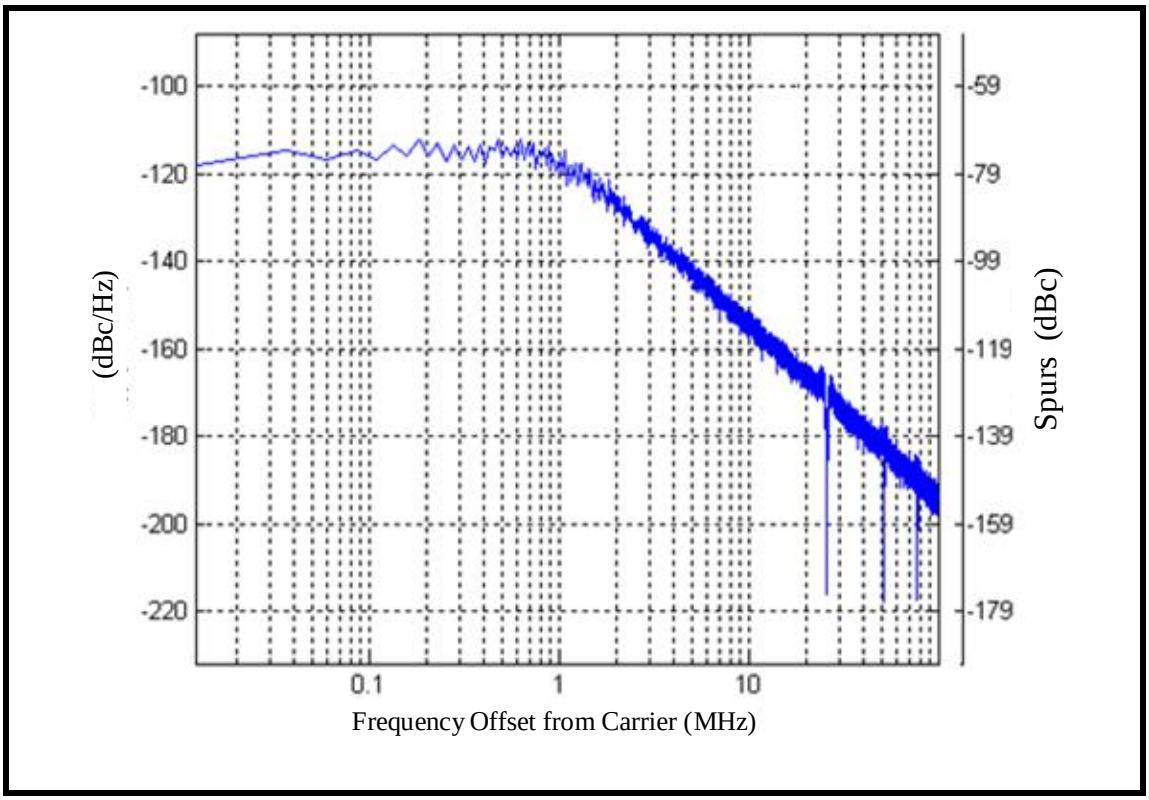

Fig. (11 a) Simulation showing the overall phase noise performance for 2nd order SD modulator.

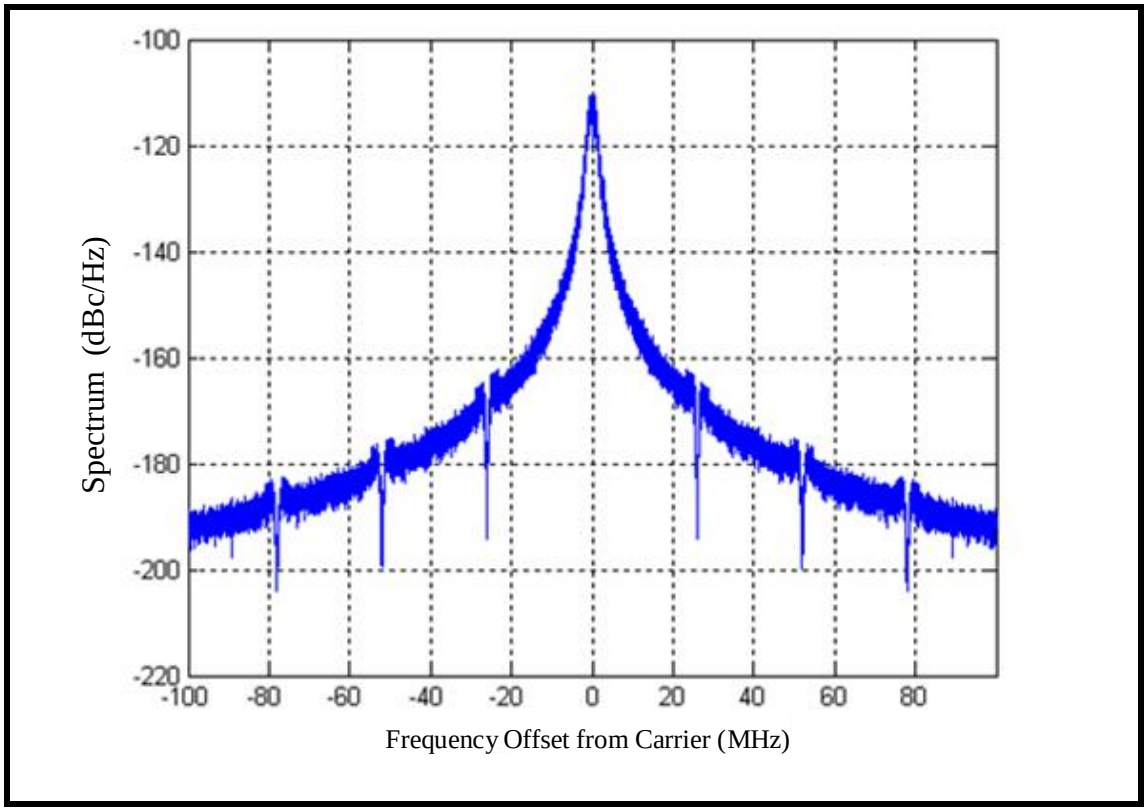

Fig. (11 b) Simulation showing the output spectrum of PLL synthesizer for 2nd order SD modulator.

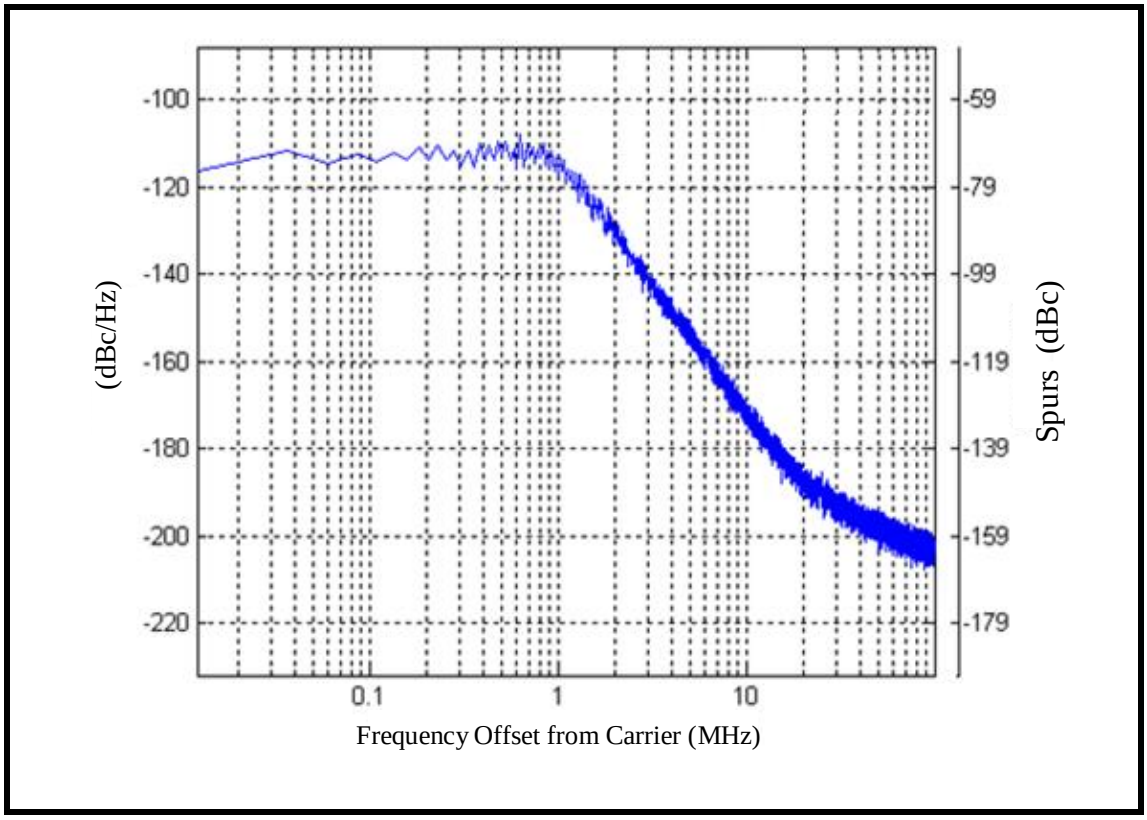

Fig. (12 a) Simulation showing the overall phase noise performance for 3rd order SD modulator.

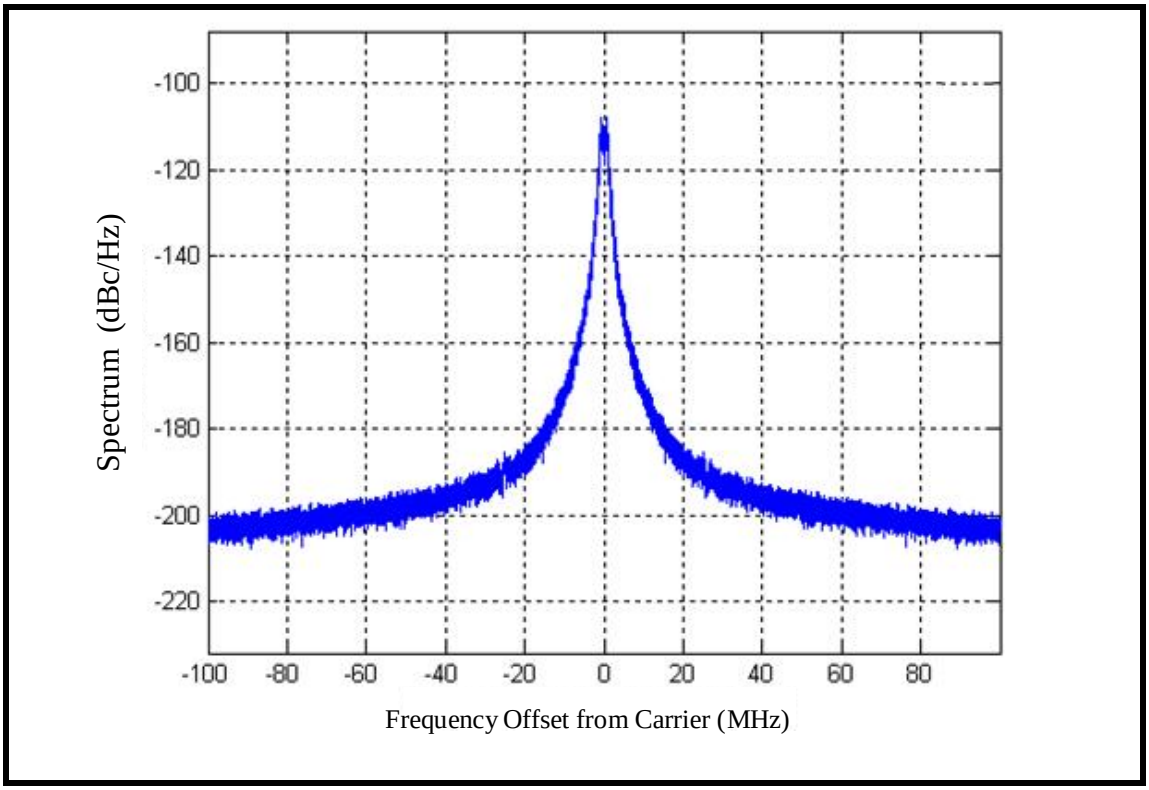

Fig. (12 b) Simulation showing the output spectrum of PLL synthesizer for 3rd order SD modulator.

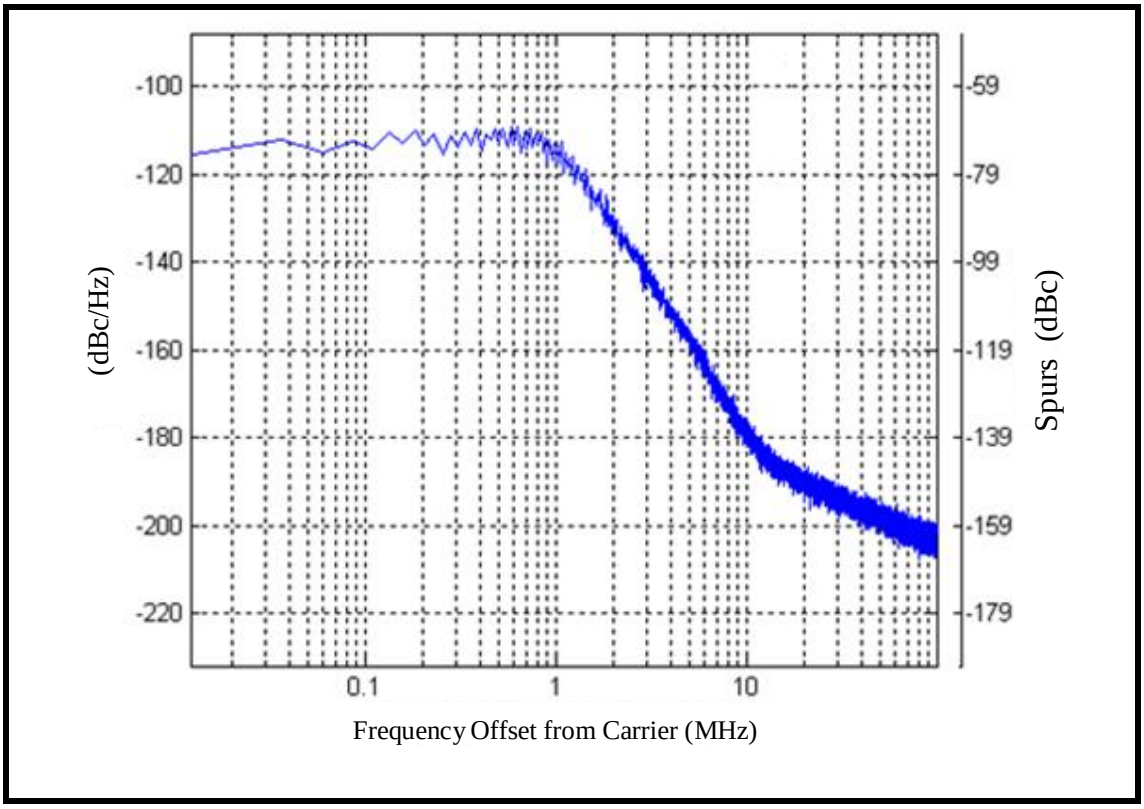

Fig. (13 a) Simulation showing the overall phase noise performance for 4th order SD modulator.

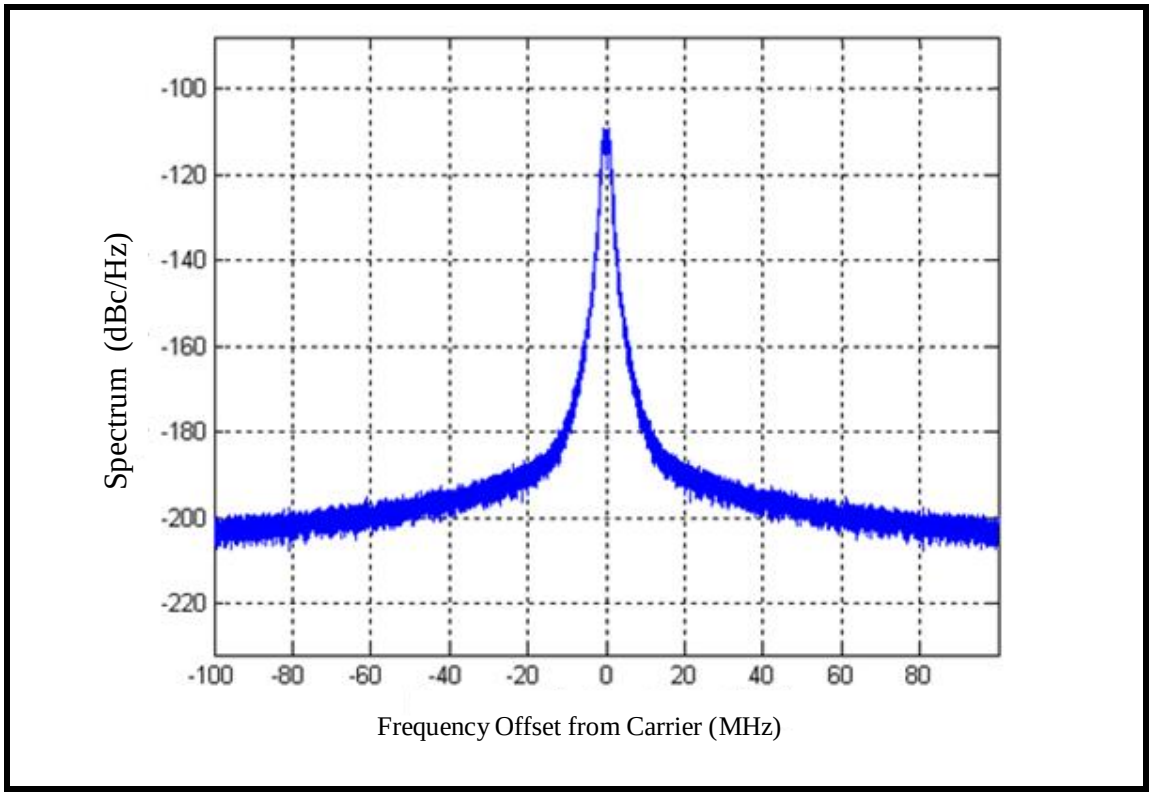

Fig. (13 b) Simulation showing the output spectrum of PLL synthesizer for 4th order SD modulator.

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الخلاصة

في هذا البحث تم مناقشة, تحليل, تصميم وتقييم المحاكاة لمضمن من النوع (ΣΔ) ومرشح دورة من الرتبة الثانية والثالثة والرابعة على التوالي لإظهار تأثيرهم على أداء مركب التردد الكسري لدائرة إقفال الطور لنظام GSM. تظهر كل نتائج المحاكاة إن النظام مستقر. النتائج التي تم الحصول عليها لمركب التردد لزمن الاستقرار ومستوى التردد الطيفي وضوضاء الطور عند (20 MHz offset) للرتبة الثانية والثالثة والرابعة لمضمن من نوع (ΣΔ) ومرشح دورة على التوالي هي 2.92 µs، -35 dBc، -164 dBc/Hz، 3.28 µs، -64 dBc، -186dBc/Hz، 3.38 µs، -79 dBc و -190 dBc/Hz على التوالي. أظهرت نتائج المحاكاة تحسين في مستوى التردد الطيفي وضوضاء الطور بمقدار -19 Bc، -31 dBc/Hz لنظام الرتبة الثالثة و -34 dBc، -35 dBc/Hz لنظام الرتبة الرابعة على التوالي إذا ماقورنت بنتائج العمل المنشورة. استخدمت الحقيبتان البرمجيتان CppSim و Matlab (R2007a) في محاكاة مركب التردد من نوع (ΣΔ fractional-N PLL).