Journal of Al-Nahrain University Science Vol.15 (4), December, 2012, pp.١٢9-١33

Electronic Properties of PbTe \ Si Hetrojunction

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Abstract

In this paper a study of the effect of annealing temperature on the electrical properties of PbTe films prepared by thermal evaporation technique on Si wafer has been achieved. The electric properties of PbTe including d.c conductivity and Hall effect, from d.c measurement. It is found that the electrical activation energies Ea_1 and Ea_2 increase from 0. 175 eV to 0.24 eV and form 0.53 eV to 0.536 eV with the increase of annealing temperature from 323 k to 373 k. Hall measurements showed that all films are p-type. Electrical properties of PbTe\Si hetrojunction, fabricated by deposition of PbTe film on Si using thermal evaporation, include current (I) and voltage (V) characterizations under dark and illumination conditions and capacitance and voltage measurement at varying annealing temperatures.

Capacitance (C) and voltage (V) characteristics showed that the fabricated diode type. The built in potential was determined by extrapolation of $1/C^2$-V curve. The built in potential (V_{bi}) for the PbTe\ Si System was found to be increase from 1.37eV to 1.65eV with increasing of annealing temperature.

1. Introduction

Narrow gap semiconductors are the most sensitive materials for infrared sensors. These materials are used for thermal imaging in the 3–5μm atmospheric windows [1]. PbTe is a promising material candidate because of its superior chemical stability and the ease of film deposition. Band gap tunability can be achieved through alloying PbTe with SnTe. Different deposition techniques have been employed for PbTe film deposition, including flash evaporation and a hot-wall technique. Single crystal PbTe and $Pb_{1-x}Sn_xTe$ have been studied for the fabrication of IR photodetectors and long wavelength laser devices. Boberl *et al.* reported epitaxial PbTe detectors integrated with mid-IR filters and showed enhanced photoresponsivity at room temperature [2]. The narrow band gap IV-VI semiconductors (PbTe) have long been used for mid-infrared optoelectronic device applications [1]. Recently, high-quality epitaxial growth of Se and related materials on (111) oriented Si substrates has been accomplished by incorporating thin intermediate BaF2/CaF2 layers. Heteroepitaxial growth of PbTe on silicon takes advantage of silicon integration technology to obtain inexpensive photonic devices. PbTe layers grown heteroepitaxially on Si (111) have been fabricated [3]. In this paper we will present deposition PbTe thin film fabricated by the thermal evaporation technique. Lead salts and their alloys have a number of interesting physical properties as well as numerous potential applications [4].Lead chalcogenides (PbS, PbSe and PbTe) exhibit some unusual and unique properties such as high dielectric constant and high mobility[5]. IV-VI compounds have found a new sphere of applications due to the development of laser technology. Laser diodes based on lead chalcogenides and their alloys act as an important source of tunable radiations in mid infra-red wavelength region [6].

2. Experimental Work

Substrates of n-type single crystal Si wafers of resistivity 3(Ω-cm) and orientation (111) were used in the present study. After scribing these wafers into small pieces (typically 1cm x 0.6cm in size), with one surface polished with 2HF: $3HNO_3$: $3CH_3COOH$ mixture (3:5:3), were cleaned ultrasonically by dipping in distilled water, acetone and isopropyl alcohol alternately. After cleaning, the samples were oxidized in dry oxygen [7]. The films of PbTe were prepared by thermal evaporation in vacuum of the order of 10^{-5} torr, with a rate of evaporation ≈0.8 nm/min, onto clean silicon mirror-like side substrates at room temperature (~300K). The average thicknesses of the deposits were determined by microbalance method. The maximum error in the determination of thickness was of the order of 10% estimated for the thinnest films (PbTe\Si films of thickness 350 nm).Ohmic contacts of Al was evaporated on the silicon side and PbTe side for Study the Electrical Properties PbTe\Si Heterojunction [8].

3. Results and Discussion

3.1 Electrical Properties of PbTe Films

3.1.1d.c conductivity of PbTe layer

In order to study conductivity mechanisms, it is convenient to plot logarithm of the conductivity (lnσ) as a function of 1000/T for PbTe films over the range (303 – 483) K for different annealing temperatures, as shown in figure1. It is clear from this figure that there are two transport mechanisms, giving rise to two activation energies E_{a1} and E_{a2}. At higher temperature range (363–483) K, the conduction mechanism is due to carrier excited into the extended states beyond the mobility edge. At lower temperature range (303 – 483) K; the conduction mechanism is due to carrier excited into localized states at the edge of the band.

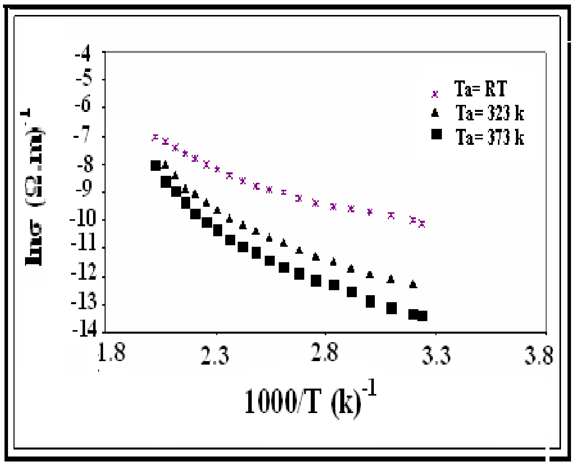

Fig.(1) lnσ as a function of 1000/T for PbTe films.

Table (1)
d.c conductivity parameters for PbTe films at annealing temperatures.

T_a (K)	E_{a1} (eV)	Temp. Range (K)	E_{a2} (eV)	Temp. Range (K)
R.T	0.14	303-363	0.44	363-483
323	0.175	303-363	0.53	363-483
373	0.24	303-363	0.536	363-483

Table (1) shows the effect of annealing temperatures on (Ea_1, Ea_2) at (T_a=323 and 373K) for PbTe. It is found that the activation energy tends to increase with the increasing of the annealing temperature. This increase is obviously due to the increasing in the energy gap, which may be due to the dense in the valence band (V.B) & condition band (C.B). The effect is shown clearly by the improvement in crystallinity during annealing (see Fig.(1)).

3.1.2 Hall Effect

The type of charge carriers, carrier concentration (n_H) and Hall mobility (μ_H) of charge carriers have been estimated from Hall measurements. The variation of Hall voltage with the current for PbTe films deposited at room temperature (R.T) for different annealing temperatures are shown in Fig.(2).

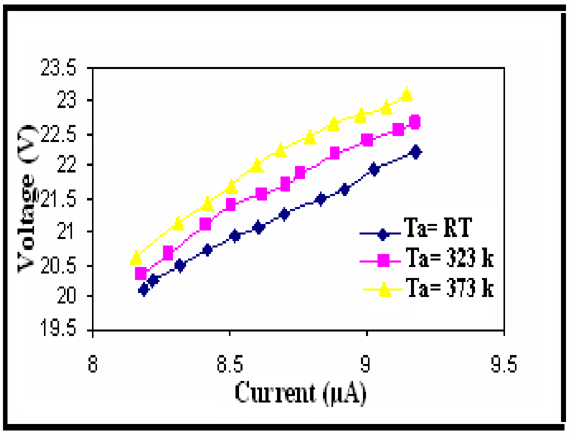

Fig.(2) Variation of Hall voltage versus current for PbTe films at annealing temperatures.

We can notice from this figure that the films of all annealing temperatures have a positive Hall coefficient observed from these figures that both the carrier's concentration and mobility decrease with increasing of annealing temperatures. This behavior is caused by either increasing the trapping centers or the films have a large amount of adsorbed oxygen which reduces both the number of charge carriers and their mobility essentially because of the higher grain boundary barrier height.

Table (2)
Hall parameters for PbTe films at different annealing temperatures.

T_a (K)	$n_H \times 10^{16}$ (cm^{-3})	$\mu_H \times 10^{-6}$ ($\frac{cm^2}{V.sec}$)
R.T	8. 55	21
323	7. 39	3.99
373	5. 6	2

3.2 Electrical Properties of PbTe\ Si Heterojunction

3.2.1 C-V Characteristics

The junction capacitance measured as a function of bias voltage for the p-PbTe\ n-Si diodes shows $(1/C)^2$ - V dependence. Fig.(3), indicate an abrupt junction in that case. According to the distances during which the transition from one region to the other is completed near the interfaces. The built - in potential (V_{bi}.) for the p-PbTe\ n-Si system was found to increase with increasing of annealing temperature

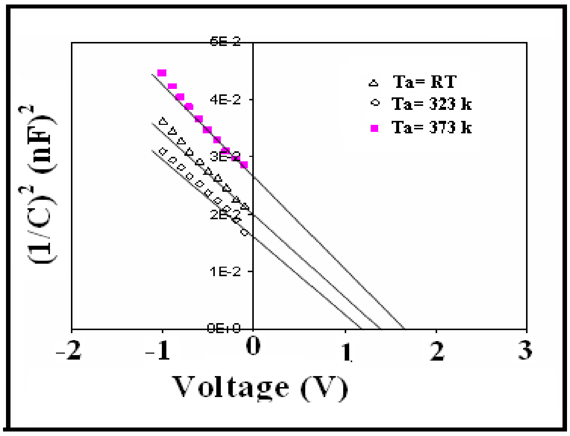

Fig.(3) 1/C² as a function of reverse bias voltage and at different annealing temperature.

Table (3)
Values of V_{bi} for PbTe \ Si hetrojunction with annealing Temperature.

Annealing Temp (K)	V_{bi}(eV)
R.T	1.91
223	1.37
373	1.65

3.2.2 I-V Characteristics for PbTe\ Si Heterojunction under Dark

One of the important parameters of a heterojunction measurement is a current-voltage characteristic which explains the behavior of the resultant current with the applied forward and reverse bias voltage. Fig.(4) shows I-V characteristic for PbTe\Si heterojunction at forward and reverse bias voltage for different annealing temperatures. In general the forward dark current is generated due to the flow of majority carriers and the applied voltage injects majority carriers which lead to the decrease of the built-in potential, as well as the width of the depletion layer. We also observed that the current increases slightly with the increase of annealing temperature due to rearrangement of the interface atoms and reduction of the dangling bond, surface states and dislocation at interface layer between PbTe and Si which leads to improvement of the junction characteristics.

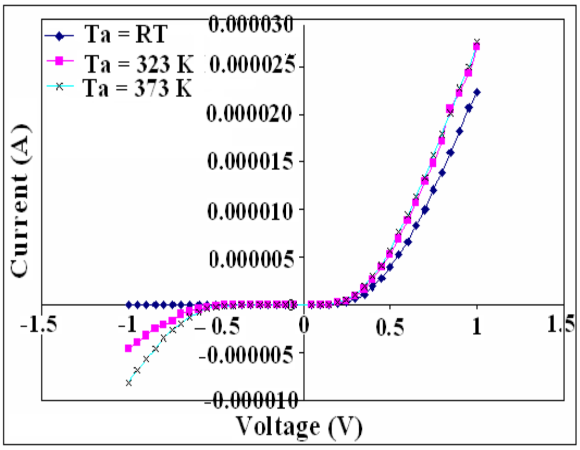

Fig.(4) I-V characteristics in the dark for PbTe\ Si heterojunction at forward and reverse bias voltage at different annealing temperatures.

3.2.3 I-V Characteristic for PbTe \ Si Heterojunction Solar Cell under Illumination

The relation between the photocurrent density (J_{ph}) and bias voltage (V) of the PbTe \ Si diodes at different thicknesses and annealing temperatures are presented in Fig.(5). The measurements were carried out under power densities equal to 60 mW/cm^2.

From this figure we observe that the photocurrent density increases with increasing of the bias voltage. We can observe from Fig.(5) that the photocurrent density increases with increasing annealing temperature and this is attributed to the increasing in the grain size, reduction of the grain boundaries and improvement of structure which leads to the increase of the mobility and increase the photocurrent density as well as the increase of the depletion width which leads to an increase of the creation of electron-hole pairs

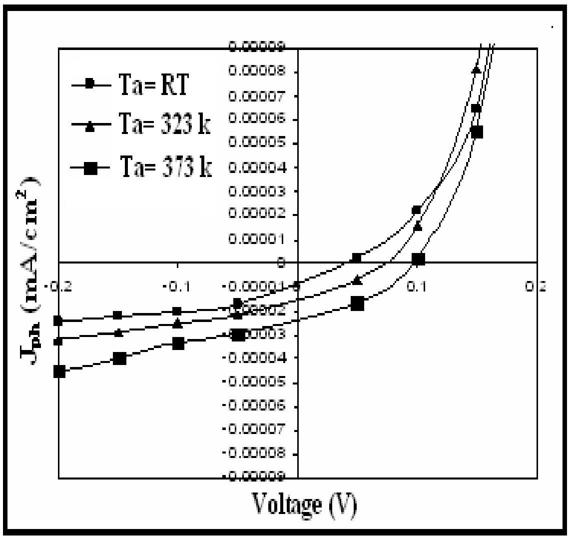

Fig.(5) I-V characteristics under Illumination for PbTe\ Si heterojunction at forward and reverse bias voltage at different annealing temperature.

4. Conclusions

4.1 Electrical Properties of PbTe Films

a- The D.C conductivity for all films decrease with increasing annealing temperatures.

b- The activation energies increase with increasing the annealing temperatures.

c- Hall measurements show that all the films are p-type. The Hall mobility and carrier concentration decrease with increasing of annealing temperatures.

4.2 Heterojunction Characteristics

4.2.1 C-V Measurements

The value of built – in potential for PbTe\Si heterojunction increases with increasing of annealing temperatures.

4.2.2 I-V Measurements

Short circuit current density (J_{sc}), open circuit voltage (V_{oc}) increase with increasing annealing temperatures.

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الخلاصة

في هذا البحث تم دراسة تأثير التلدين على الخواص الكهربائية للغشاء PbTe والمحضر بتقنية التبخير الحراري والتي تتضمن التوصيلية المستمرة وقياسات هول حيث تبين من قياسات التوصلية المستمرة أن طاقة التنشيط الكهربائية $(Ea_1),(Ea_2)$ تزداد من 0.175 إلى 0.24 الكترون فولت ومن 0.53 إلى 0.536 إلكترون فولت بزيادة درجات حرارة التلدين 323k الى 373k ومن قياسات تأثير هول تبين ان جميع الأغشية هي من نوع p-type ولجميع درجات حرارة التلدين .

إما الخصائص الكهربائية للمفرق ألهجيني PbTe/Si الناتج من ترسيب PbTe بطريقة التبخير الحراري على السليكون و تتضمن خصائص التيار – فولتية في حالة قيمة الظلام والإضاءة وخصائص سعة –فولتية وبدرجات تلدين مختلفة.

من خصائص سعة – فولتية تبين ان المفرق ألهجيني هو من النوع شديد الانحدار وان جهد البناء تم حسابه من منحنى الفولتية ومقلوب مربع السعة وتبين ان جهد البناء للمفرق الهجيني يزداد من 1.37 الى 1.65 الإلكترون فولت بزيادة درجة حرارة التلدين.