Chemical, Morphological and Electrical Properties of Porous Silicon Prepared by Photelectrochemical Etching

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Abstract

In this work, the nanocrystalline porous silicon (PS) films is prepared by photoelectrochemical etching of *n*-type silicon wafer with different currents density (20, 35 and 50 mA/cm^2) and etching time 15 min on the formation nano-sized pore array with a dimension of around few hundreds nanometric. The films were characterized by the measurement of FTIR spectroscopy and atomic force microscopy properties.Chemical fictionalization during the photoelectrochemical etching show on surface chemical composition of PS. The etching possesses inhomogeneous microstructures that contain *a*-Si clusters (Si_3–Si–H) dispersed in amorphous silica matrix and (O-SiO, C-SiO). It is observed from the FTIR analyses that the Si dangling bonds of the as-prepared PS layer have large amount of Hydrogen to form weak (Si–H) bonds. The atomic force microscopy investigation shows the rough silicon surface; with increasing etching process (current density) porous structure nucleates which leads to an increase in the width (diameter) of surface pits. Consequently, the surface roughness also increases. The electrical properties of prepared PS; namely current density-voltage characteristics under dark, show that the pass current through the PS layer decreased by increasing the current density and etching time, due to increase the resistivity of PS layer. The PS layer shows a rectifying behaviour with different rectification ratio. C-V measurements demonstrate that the behaviour of the resulting junction is more like to Schottky junction. This study makes it clear that the charge carries depletion process occur in PS layer. Moreover, the charge carries decrease and width of depletion layer increase by increasing the current density.

Keyword: porous silicon; nanostructure; etching; FTIIR; AFM; electrical properties.

Introduction

Silicon is the main material of microelectronics at present, but it is not widely used in optoelectronics. The reason is due to the inherent nature of the indirect transition in the band-edge emission. When the visible photoluminescence (PL) of electrochemically etched porous silicon was reported by Canham in 1990, the material has been extensively studied to clarify luminescence mechanism and to investigate its possible use as a new material for the optical device application [1]. The early attempts to use porous silicon in sensing applications were based on variations of its electrical properties such as capacitance and conductivity. In addition, optical properties of porous silicon have been exploited for chemical and biological sensing due to their fast response time and relative safety for operation in hazardous environments such as flammable vapors or gases. The most popular optical techniques are based on the change of optical reflectivity, photoluminescence, birefringence, and the properties of optical waveguides [2].

Porous silicon consists of a network of nanoscale sized silicon wires and voids which formed when crystalline silicon wafers are etched electrochemically in hydrofluoric acid based electrolyte solution under constant anodization conditions. The precise control of porosity and thickness allows the tailoring of optical properties of porous silicon and has opened the door to a multitude of applications in optoelectronics technology [3].

Porous Silicon can exhibit a large variety of morphologies and particle size. It has been reported that the luminescence of the PS is ascribed to the quantum confinement effect (QCE) as well as to the presence of Si-H_n bond near the surface of nanocrystallites [4].

Experimental Procedure

The silicon samples after cleaning were immersed in electronic grade (40%) HF acid supplied from BDH Company. The immersed samples were mounted on Teflon cell and light irradiated at normal incidence on the polished side in such a way that the current required for the etching process, could pass from bottom surface to light irradiated area on the top of the polished surface through the electrolyte. Quartz tungsten halogen lamp (200W) integrated with diachronic ellipsoidal mirror supplied from *Phillips* Company was focused on a silicon wafer was fixed at 15 cm.

The commercially available n-type Si (phosphorus doped) with resistivities of (thickness 508±15µm and resistivity 1.5-4) Ω-cm and (111) orientation were employed as substrates with dimensions of 1.5x1.5 cm to prepare PS by photoelectrochemical (PCE) etching. The electrolyte was prepared by mixing HF (40%) and ethanol in 1:1 ratios. The wafer and the solution were placed in a Teflon cell. The porous layers on the surface of these samples were prepared at current densities of 10, 20, 35 and 50 mA/cm^2 with etching time of 15 min.

The porous layers on the surface of these samples were prepared at characterized Surface chemical composition of PS by FTIR IRAffinity-1 Fourier Transform I nfrared Spectrophotometer SHIMADZU, and morphological of silicon nanocrystallites by the atomic force micrographs (AFM) type AA3000 Scanning Probe Microscope Angstrom Advanced Inc.

Results and Discussion

a. Chemical Composition of PS Layer

Surface chemical composition of PS is best probed with Fourier Transform Infrared (FTIR) spectroscopy is showing Fig. (1). FTIR signal in PS is larger and easier to measure than in bulk Si due to much larger specific area.

The pore surface includes a high density of dangling bonds of Si for original impurities such as hydrogen and fluorine, which are residuals from the electrolyte. Additionally, if the manufactured PS layer is stored in ambient air for a few hours, the surface oxidizes spontaneously.

Chemical bonds and their IR resonance positions detected in PS are shown in Table (1). Our results are in good agreement with those of other investigations [5-9].

Table (1)
Wavenumber positions and attributions of the transmittance peaks observed in several PS samples by Fourier transform infrared absorption FTIR measurements.

Peak position (cm^{-1})	*Attribution*
449.31	Si-O stretching in Si-O-Si
632.65	Si-H bending in (Si_3-SiH)
867.97	Si-H_2 wagging
1045.42	Si-O stretching in O-SiO and C-SiO
1161.15	Si-O-Si symmetric stretch.
1448.54	C-H_3 asymmetric deformed
1705.07	C-O
2095.52	Si-H_2 stretch. (Si_3-SiH)
3000-3650	SiO-H

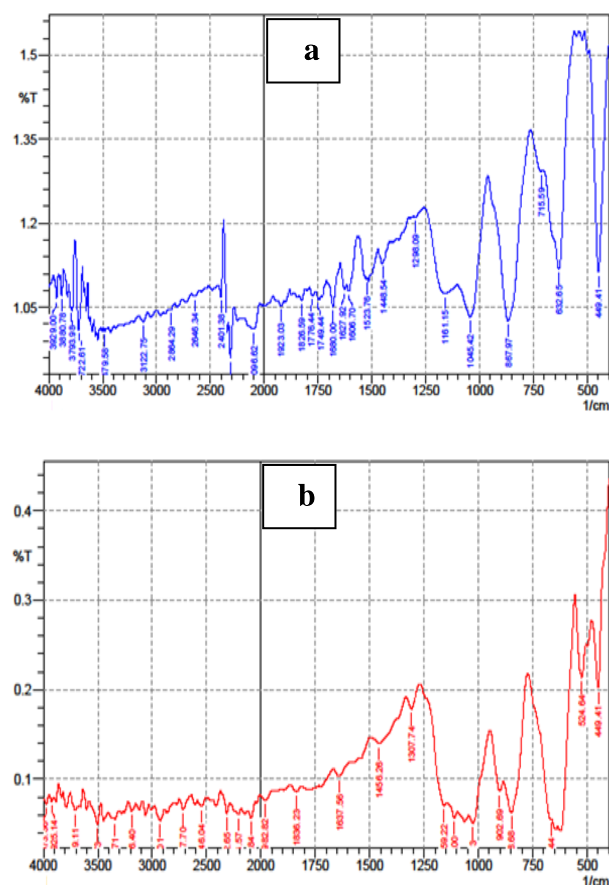
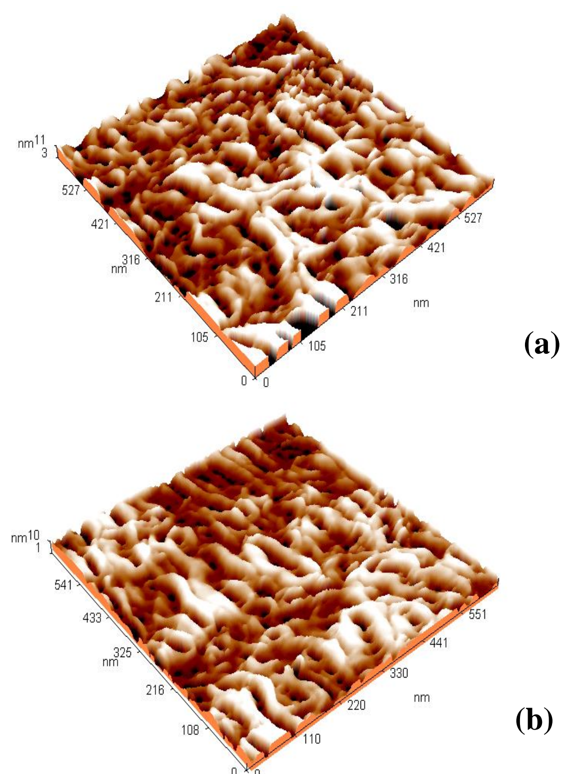


Fig. (1) IR transmittance spectrum of a PS layer (a) 20 & (b) 50mA/cm^2 at etching time 15 min.

b. Properties

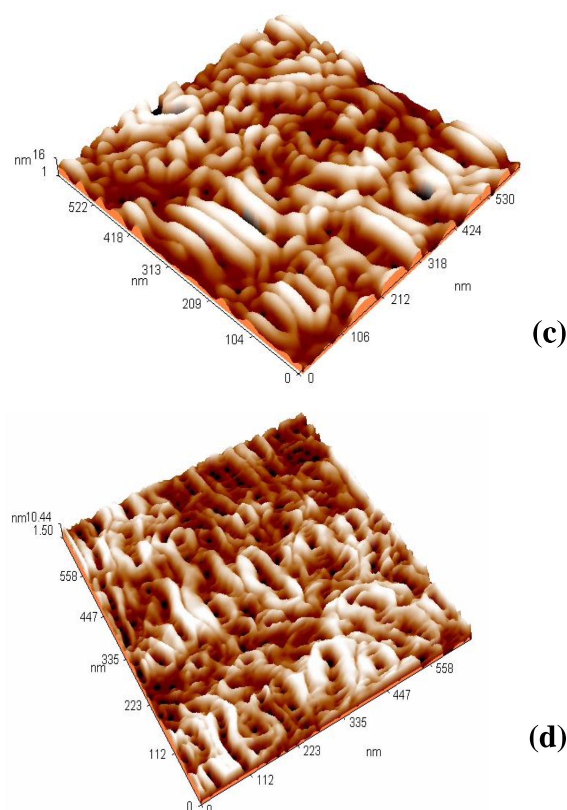
The surface morphology of the PS semiconductors is known to be very complicated and strongly depends on fabrication conditions. Therefore, the current density and etching time can be used to control the size and shape of the final structures. The morphological properties of the PS samples prepared with different current density values (10, 20, 35 and 50 mA/cm2) and etching time at 15 min are shown in Fig. (2). The pore morphology was analyzed under conditions of varying current densities. At low current density, a highly branched, randomly directed and highly interconnected meshwork of pores was obtained. However, increasing in current density orders the small pores to exhibit cylindrical shapes giving rise to larger pore diameter of surface pits. Consequently, the surface roughness also increases (see Table (2)).

It is clearly visible the porous layer consisting of many void propagating in the direction perpendicular to the surface, with numerous side branches. This property is a consequence of the formation mechanism, which consists in a plane dissolution front propagating in a direction perpendicular to the surface. The average pore diameter appears in good agreement with what expected for a meso-porous layer.



(a)

(b)



(c)

(d)

Fig. (2) 3D AFM image of meso-porous silicon monolayer prepared at current density (a) 10, (b) 20 & (c) 35 & (d) 50mA/cm² etching time 15 min.

Table (2)
The calculated morphology characteristics of PS samples prepared with different etching process.

Etching time (min)	*Current density (mA/cm^2)*	*Roughness Ave. (nm)*	*Ave. Diameter (nm)*
15	10	2.17	16.82
	20	2.25	19.05
	35	3.57	23.41
	50	2.05	27.62

c. Electrical properties

I-V Characteristics in dark

Fig.(3), a typical diode behavior can be seen. This figure shows the current density-voltage characteristics of Al/PS/n-Si/Al sandwich structure device prepared at 20 min, with different current densities (10, 20, 35 and 50 mA/cm^2). The J-V curves were obtained by applying a various applied bias (sweeping from -5 V to +5 V) and then measuring the resulting current. By increasing the current density from 10 to 50 mA/cm^2, it is observed smaller current passing through the PS layer with the same applied voltage. This decrease current values reflect the fact which is, increasing the current density leads to increase the porosity and then the resistivity which leads to decrease the passing current.

The onset of forward current density is found to be about (~1V). Under reverse bias conditions, the current density is significantly low, and even to be zero. The characteristics show rectifying behavior.

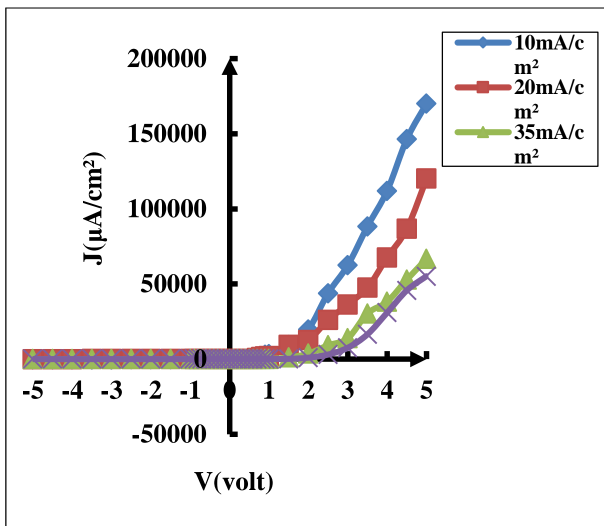


Fig.(3) The Current density – Voltage characteristics of PS prepared under different current densities and etching time (15 min).

Photocurrent density –voltage characteristics

Fig. (4) represents the J-V characteristics in dark and under different power intensities (5, 20, 60, and 120mW/cm^2) at room temperature of Al/PS/p-Si/Al sandwich structure device, containing PS layers prepared at 20 min, with different current densities (10, 20, 35 and 50 mA/cm^2). The photocurrent curves were obtained by applying a various the applied reverse bias (sweeping from -2 V to 0 V) and then measuring the resulting current.

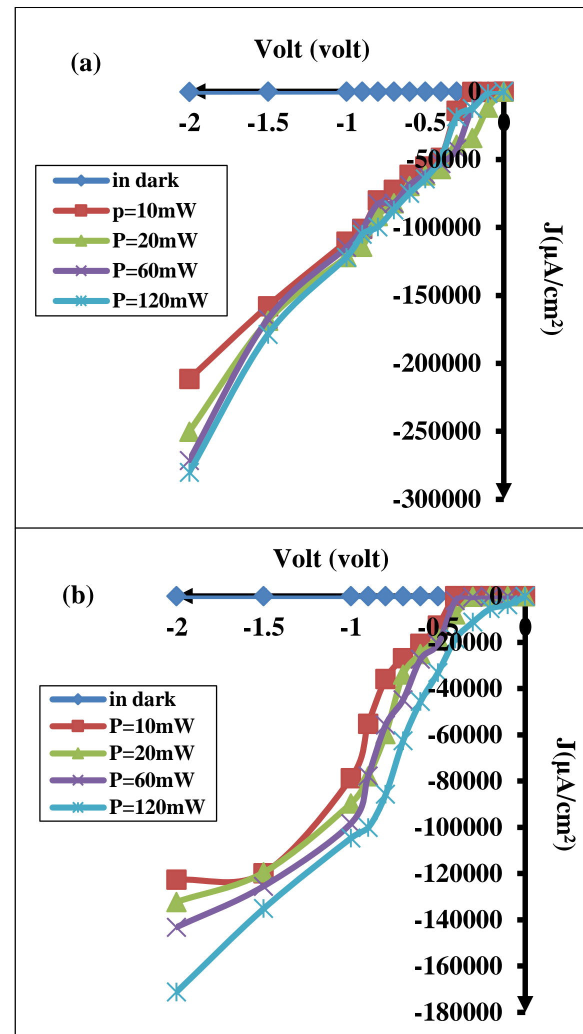


Fig. (4) Photocurrent density – voltage characteristics of PS prepared with different current densities (a) 10 and (b) 50mA/cm2 at etching time 15 min.

Fig. (4) represents the *J-V* characteristics in dark and under different power intensities (10, 20, 60, and 120 mW/cm^2) at room temperature of Al/PS/p-Si/Al sandwich structure device, containing PS layers prepared at 15 min, with different current densities (10, 20, 35 and 50 mA/cm^2). However the relation of the J-V curves refers to photo-generated carriers and associated light absorption takes place in the depletion region. When the structures are illuminated, the electron-hole pairs generated in the depletion layer of PS/crystalline silicon heterojunction would reduce the barrier for the electrons [10].

In forward bias this will have no effect since the current may be limited by the porous layer resistance.

Capacitance – voltage (*C-V*)

The capacitance-voltage (*C-V*) characteristics of Al/PS/n-Si/Al sandwich structure device depend on the morphology and the porosity of the etched silicon surface. Fig. (5) shows the *C-V* characteristics of the sandwich structure with different etching current densities (10, 20, 35 and 50mA /cm^2), and constant etching time at 15 min.

The effect of the etching current density on the *C-V* characteristics is studied. Results in Fig.(6), shows that the increase of the etching current density decreases the capacitance of the PS layer. This behavior was attributed to the increase of the depletion region width which leading to the enhancement of built-in potential.

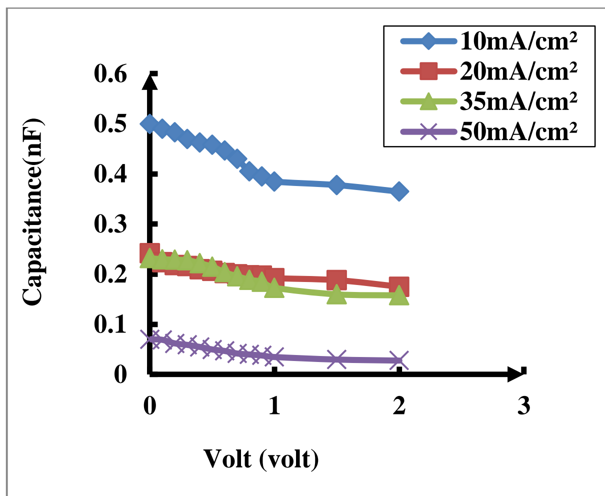
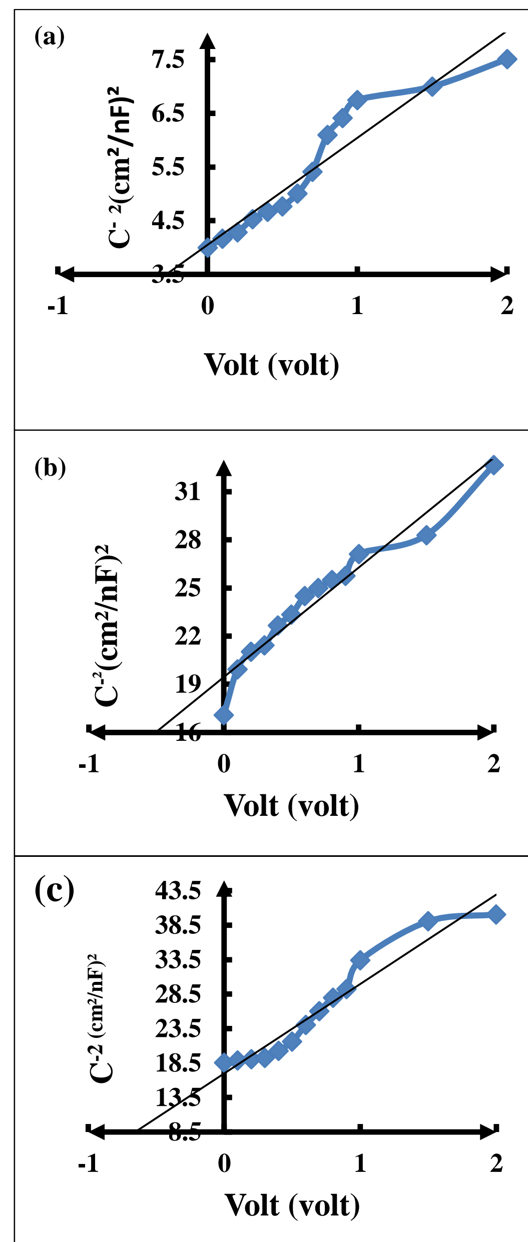


Fig (5) C-V characteristics of PS prepared with different current densities (10, 20, 35, and 50mA/cm²), and fixed etching time at (15min).

The relation between inverse capacitance squared against the reverse bias is shown in Fig.(6). This exponential relationship represents that the junction was an abrupt type. According to the C-V measurements, the built-in potential, which is calculated from this curve, the carriers concentration and the width of the depletion layer are listed in Table (3).

Table (3)
The calculated built-in potential, effective charge carrier, and width of depletion layer of PS samples prepared at different current densities.

current density (mA/cm^2)	*Etching time (min)*	*built-in potential (volt)*	*effective charge carrier (cm^{-3})*	*Width of Depletion (μm)*
10	**15**	**0.26**	**1.5 x10^{14}**	**0.14**
20		**0.5**	**4.5 x10^{13}**	**0.37**
35		**0.64**	**2.3 x10^{13}**	**0.59**
50		**0.22**	**5.1 x10^{11}**	**2.3**



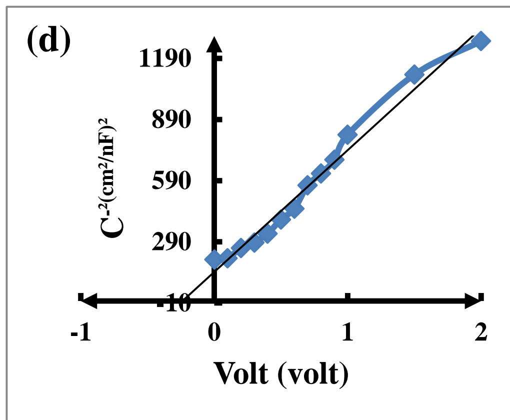


Fig.(6) The Capacitance - Voltage characteristics of PS prepared with different current density,
(a) 10, (b) 20 (c) 35 and (d) 50mA/cm2 at constant etching time (15 min).

Conclusions

1. From FTIR in porous silicon, as-prepared samples, Si-H groups (x = 1, 2 or 3) dominate over oxygen is normally.
2. The atomic force microscopy investigation shows the rough silicon surface with increasing in current density orders the small pores to exhibit sponge like giving rise to larger pore diameter.
3. The electrical properties study reveals that to:
   - The porous layer resistivity is much larger than that for crystalline silicon and this resistivity increases with increasing the current density.
   - The *C-V* characteristics shows that the increase of the current density decreases the capacitance of the PS layer. This behavior was attributed to the increasing in the depletion region width which leading to the increasing of built-in potential.

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الخلاصة

في هذا البحث تم تحضير أغشية السليكون المسامي النانوية بطريقة التنميش الفوتوكهروكيميائي لرقائق السليكون من النوع المانح مع كثافة تيارات (20 و 35 و 50 ملي امبير/ سم2) لتكوين حفر بأحجام نانوية منظمة بحدود مئات قليلة من الأبعاد النانومترية وزمن تنمش ثابت 15 دقيقة وتم تشخيص الأغشية من مطيافية تحويلات فورير للأشعة تحت الحمراء وخواص مجهر القوى الذري. حيث تم تحديد المجاميع الفعالة الكيميائية خلال التنميش الكهروكيمياوي التي تظهر على سطح المركب الكيميائي للسليكون المسامي. ان عملية التنميش الكهروكيميائية الضوئية التي تحوي على تراكيب غير متجانسة في السليكون العشوائي مثل عناقيد $(Si_3\text{-}Si\text{-}H)$ وعلى مجموعات (O-SiO, C-SiO) المشتتة في السليكا العشوائية. من تحليلات تحويلات فورير للاشعة تحت الحمراء أظهرت أواصر السليكون المتدلية لطبقة السليكون المسامي كما تم ترسيبها حيث تحوي كمية كبيرة من الهيدروجين على شكل أواصر (Si-H) الضعيفة.

أظهرت اختبارات مجهر القوى الذري على سطح السليكون ان نوى البنية المسامية التي تؤدي إلى زيادة في عرض (القطر) حفر السطح مع زيادة عملية التنميش (كثافة التيار). وبالتالي فإن الزيادة بخشونة السطح أيضا تزداد.

الخصائص الكهربائية لطبقة السليكون المسامي المحضرة؛ اي خصائص تيار – جهد تحت الظلام، أظهرت ان التيار المار خلال طبقة السليكون المسامي يقل بزيادة كثافة التيار وزمن التنميش، نتيجةً لزيادة مقاومية طبقة السليكون المسامي. أوضحت طبقة السليكون المسامي سلوكاً تقويمياً مع نسب تقويم مختلفة. أظهرت قياسات سعة – جهد ان سلوك الوصلة الناتج اشبه بكثير بوصلة شوتكي. هذه الدراسة بينت حدوث عملية استنزاف لحاملات الشحنة في طبقة السليكون المسامي. علاوةً على ذلك، نقصان حاملات الشحنة وزيادة عرض منطقة الأستنزاف يحدث بزيادة كثافة التيار.