

This converter is tested by assuming V_d constant. Therefore, L and C are calculated according to these equations:[3]

$$I_{LB,max} = \frac{TsV_d}{8L}$$

$$\therefore \frac{\Delta V_o}{V_o} = \frac{1}{8} \frac{Ts^2(1-D)}{LC} = \frac{\pi^2}{2} (1-D) \left(\frac{fc}{fs} \right)^2$$

These two equations parameters are calculated according to the PV panel model ($I-V$) curve shown in Fig.(2). $V_{PV} = V_d = 19.8V$ at $2.4A = I_{LB,max}$ therefore $L \approx 52\mu H$ while $C \geq 30\mu F$ (for percentage ripple less than 8% and $D = 0.6$ at continuous mode condition).

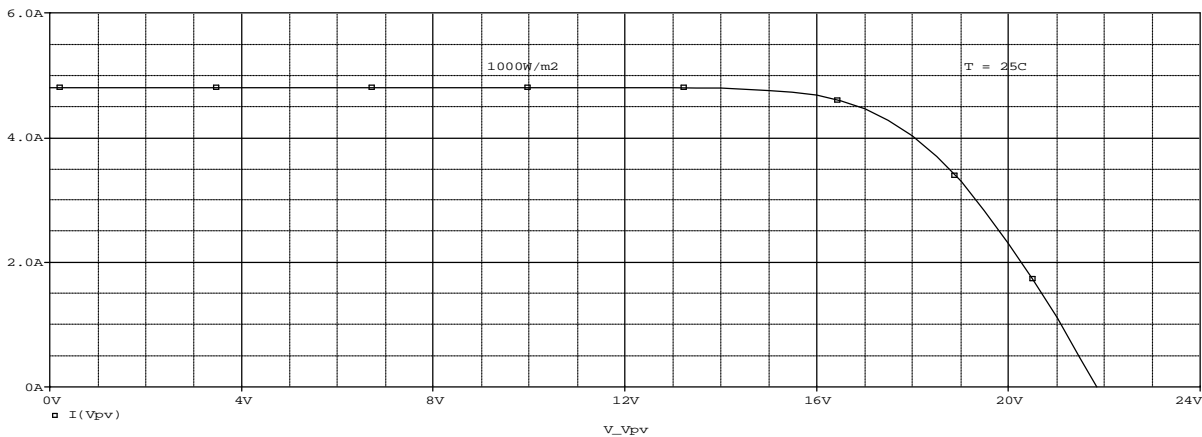


Fig.(2) : The ($I-V$) characteristics of the PV panel.

The buck converter can match the load to the PV panel if the load is less than the optimum load for the PV panel [4]. The output diode D1 (BA204) conducts when the power switch turns OFF and provides a path for the inductor current. An important criterion for selecting the rectifier includes fast switching, breakdown voltage, current rating and low forward voltage drop to minimize power dissipation. The best solution for low voltage drop is usually a Schottky rectifier.[5]

Also, it should be noted that the input current (PV current) for the buck converter is of discontinuous (switching) nature. This results in an unstable operating point on PV panel which switches between maximum power point and the open circuit and results in the loss of energy. Under such condition true maximum power point operation could never be achieved. To avoid this problem a large capacitor C1 is used at the input of the buck converter unit. This offers a stable operating point on the PV panel. The capacitor still introduces a switching frequency ripple on the PV panel voltage because of charging and discharging in every cycle. This ripple can be kept to a minimum acceptable value by using a

large capacitor at the input. A $2000\mu F$ capacitor gives the satisfactory results.[4]

PWM Generator

This unit shown in Fig.(3) generates the signal with necessary duty ratio to drive the switching devices of the converter. The error amplifier U10 (LM324) detects the error output results from the difference between the reference voltage (V_{ref}) and the actual voltage (V_{fb}); this error level is applied to the control terminal (pin5) of the 555 timer.

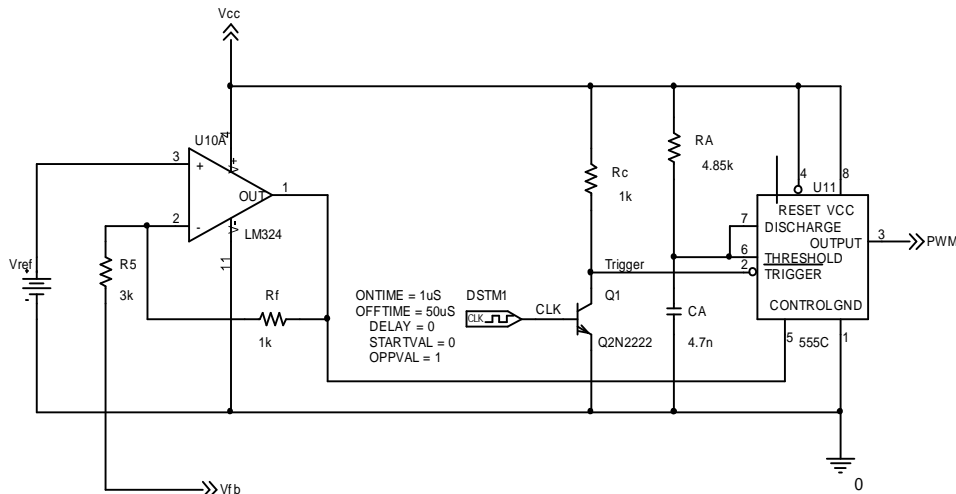


Fig.(3) : The whole system of the PWM generator.

The 555 timer is operated in monostable mode. Triggering the 555 timer in monostable mode with a continuous sequence of pulses allows the output pulse width to be modulated by changing the amplitude of a signal applied to the control input pin5. Trigger signal on pin2 causes the 555 timer output signal to go high. Retriggering will occur if the trigger pulse is hold low longer than the 555 timer output pulse width. To achieve this action the transistor Q1 (2N2222) is connected as explained in Fig.(3), to raising the voltage level of the trigger terminal pin5 and prevent the 555 timer to stop. The resistor R_A and the capacitor C_A limited the output pulse width for 555 timer. These two elements are calculated according to the equation below;

$$T_{on} = 1.098 R_A C_A$$

For $T_{on} = 25\mu s$, let $C_A = 4.7nF$ then $R_A = 4.85k\Omega$.

MOSFET Gate Drive Circuit

The output of the PWM signal is applied to the OP amplifier U19 (LM311) shown in Fig.(4). This OP amplifier supplied pulse of sufficient voltages and drove current to the gate of the switching device M1 (M2N6755) through a resistance R_g . The OP amplifier.

U19 represents the buffer circuit between the PWM generator and the gate of the MOSFET switch, the output of the gate drive act as open collector terminology. For this reason the resistor R_{c1} is connected between V_{cc} and the output terminal of U19 to get the train of pulses. In the same manner OP amplifier U23 (LM311) is used to drive the second MOSFET M2 (M2N6755).

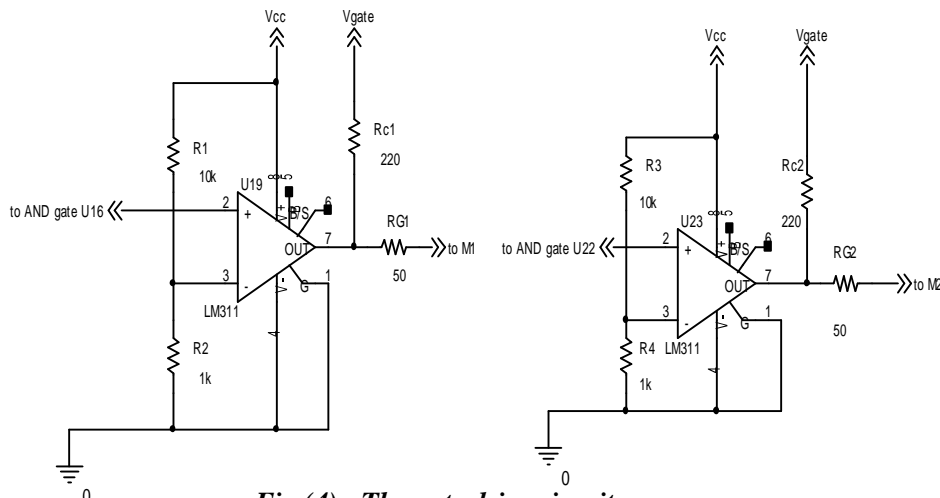


Fig.(4) : The gate drive circuit.

Sources Control Circuit

The circuit shown in Fig.(5) represent the D-multiplexer logic circuit and there elements are U18A (CD4081B), U20A (4009A) and

U21A (4001B). This circuit performs the interchange between two sources (PV panel and battery). When V4 equal zero the PV panel is active otherwise the other.

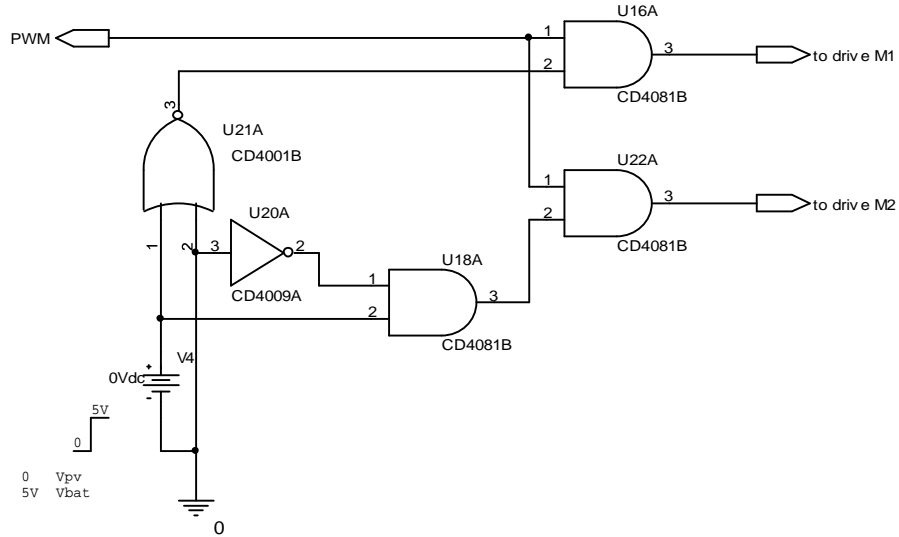


Fig.(5) : The sources control circuit.

Two Input Buck Converter Simulation Results

In this section, the waveforms obtained from transient simulation of buck converter for different modes of operation, boundary continuous and discontinuous, are presented.

Transient simulation of the converter system was carried out in Orcad Pspice Simulator. The circuit schematic of the buck converter system is given in Fig (6).

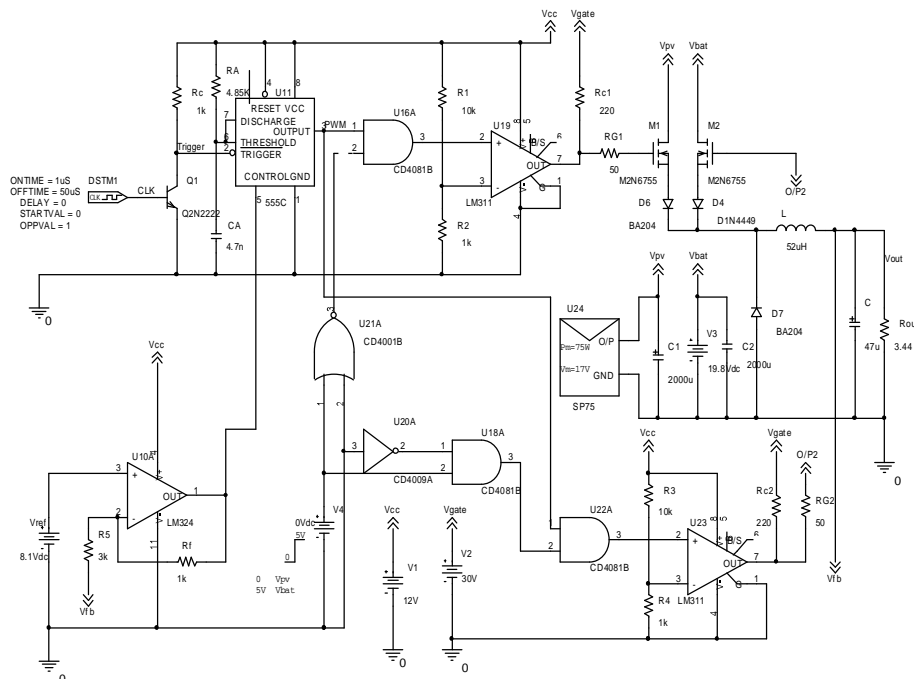


Fig. (6) : The complete circuit of two input PWM buck converter.

The simulation waveform for a buck converter operates in the boundary modes are displayed in Fig.(7) through 12. Fig.(7) gives the output voltage and current of the converter

from the PV pspice model. Also Fig.(8) gives the output voltage and current of the converter but from the battery. It is observed that the output voltage is equal to 8.5V and the output current equal to 2.4A in the two cases.

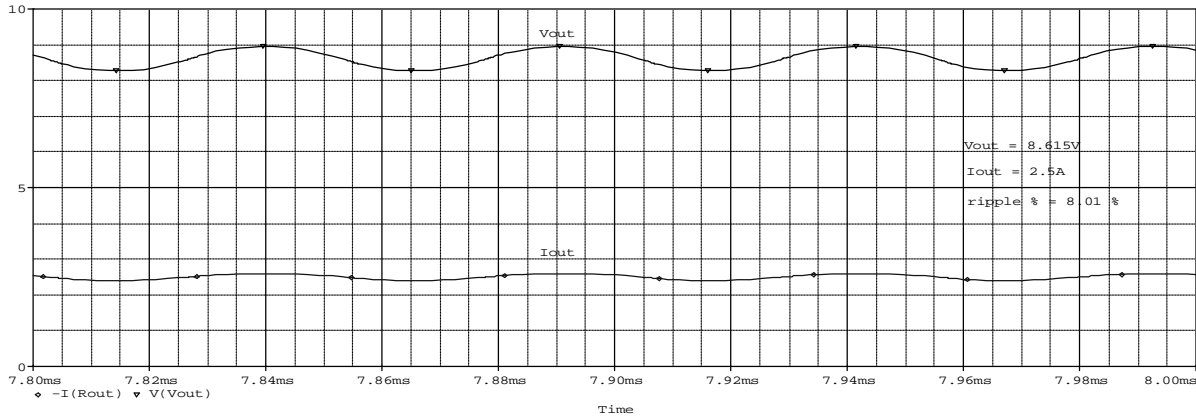


Fig.(7): The waveform patterns in boundary represent V_{out} , I_{out} in case of PV panel is on, $D=0.5$.

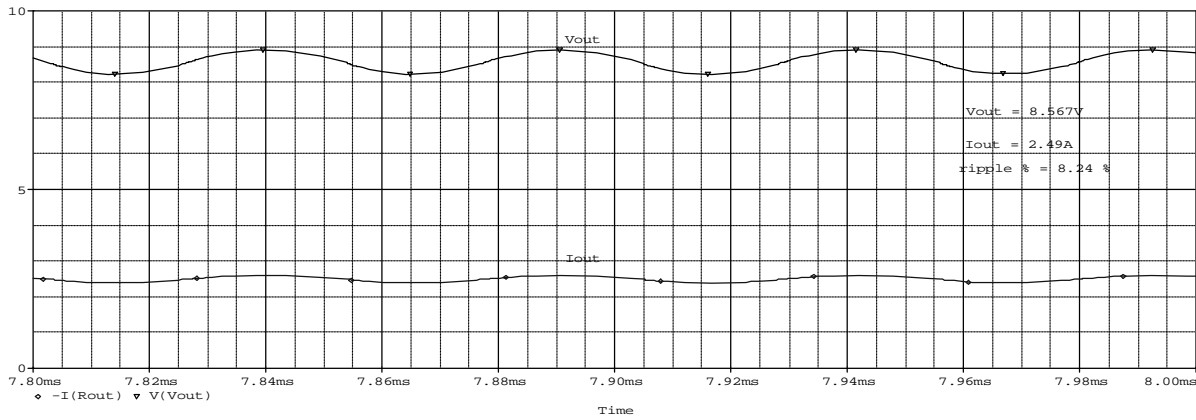


Fig.(8) : The waveform patterns in boundary represent V_{out} , I_{out} in case of battery is on, $D=0.5$.

The inductor voltage and current waveforms can be seen in the Figs. (9&10) for PV pspice model and a battery respectively. The trigger signal of the 555 and its output (PWM signal) are shown in Fig.(11) for PV and Fig.(12) for battery.

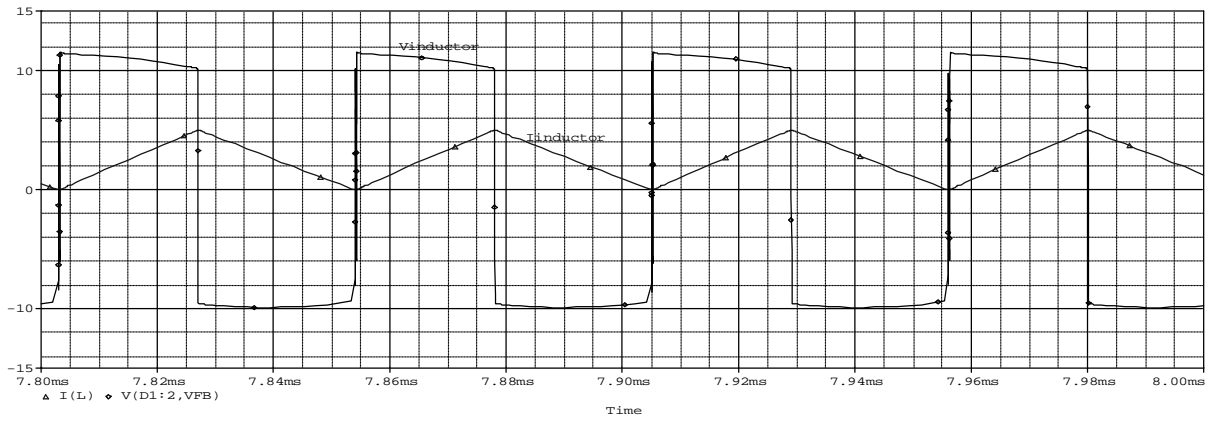


Fig.(9) : The waveform patterns in boundary represent $V_{inductor}$, $I_{inductor}$ in case of PV panel is on, $D=0.5$.

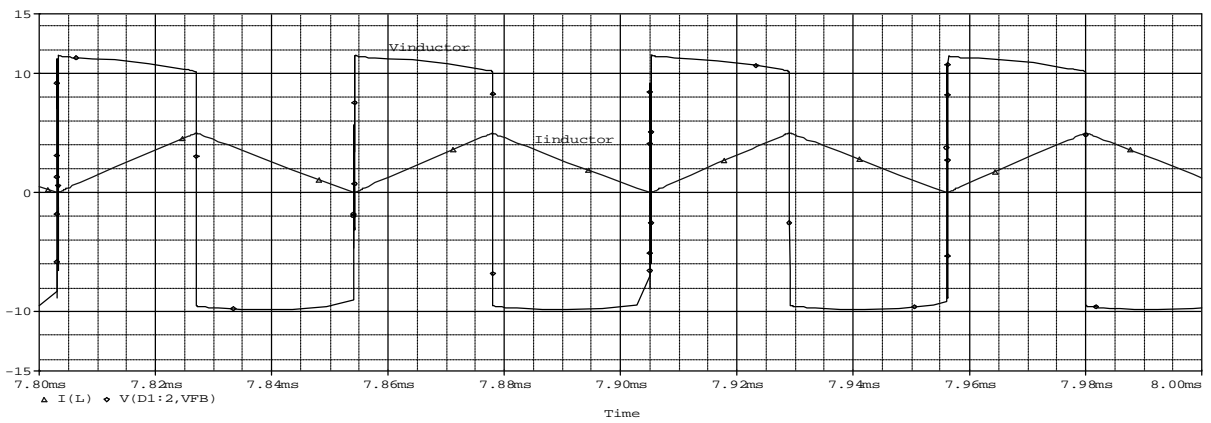


Fig.(10) : The waveform patterns in boundary represent $V_{inductor}$, $I_{inductor}$ in case of battery is on, $D=0.5$.

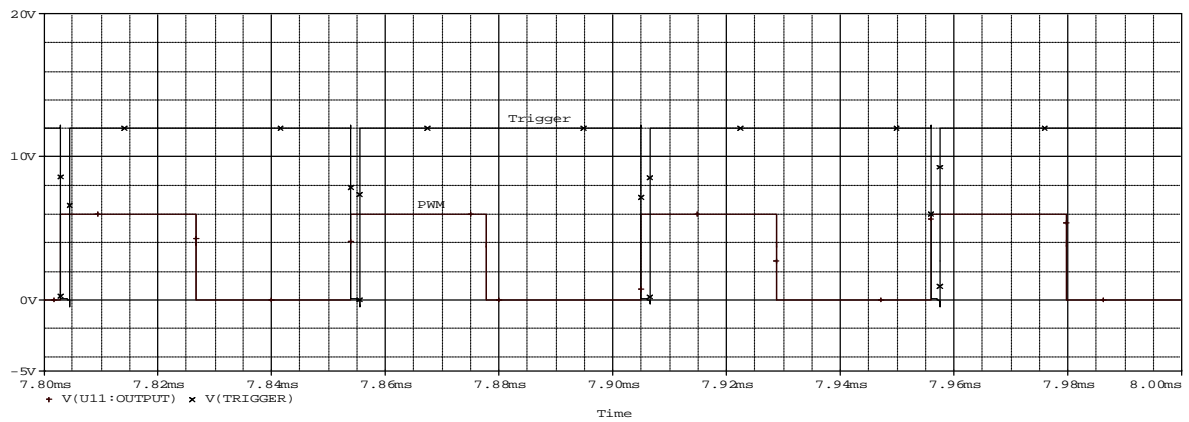


Fig.(11) : The waveform patterns in boundary represent $V_{trigger}$, V_{pwm} in case of PV panel is on, $D=0.5$.

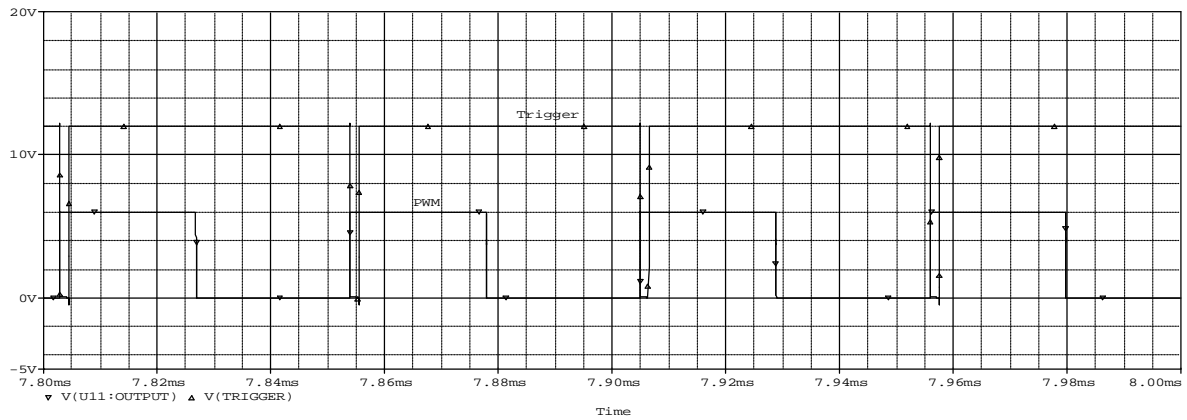


Fig.(12) : The waveform patterns in boundary represent $V_{trigger}$, V_{pwm} in case of battery is on, $D=0.5$.

In a similar manner the simulation results and discontinuous modes are explained in Fig.(13) through 24.

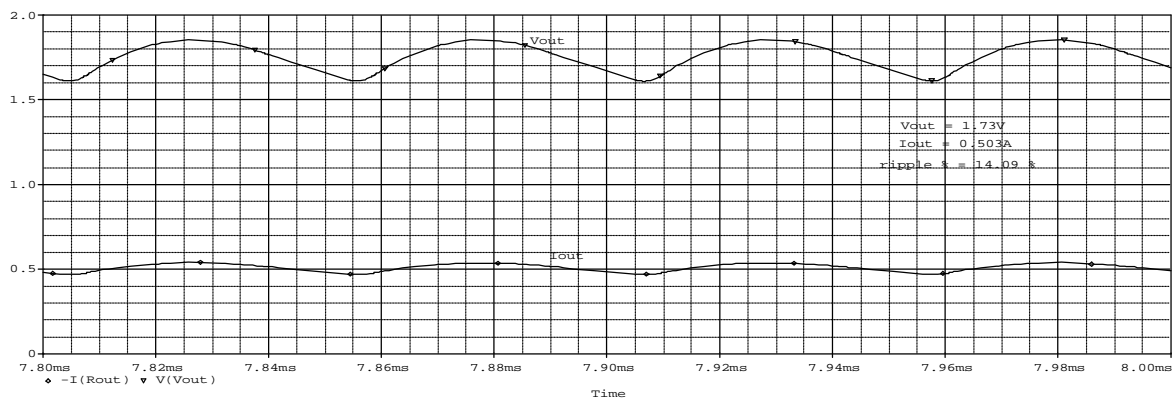


Fig.(13) : The waveform patterns in discontinuous conduction mode for V_{out} , I_{out} in case of PV panel is on, $D<0.5$.

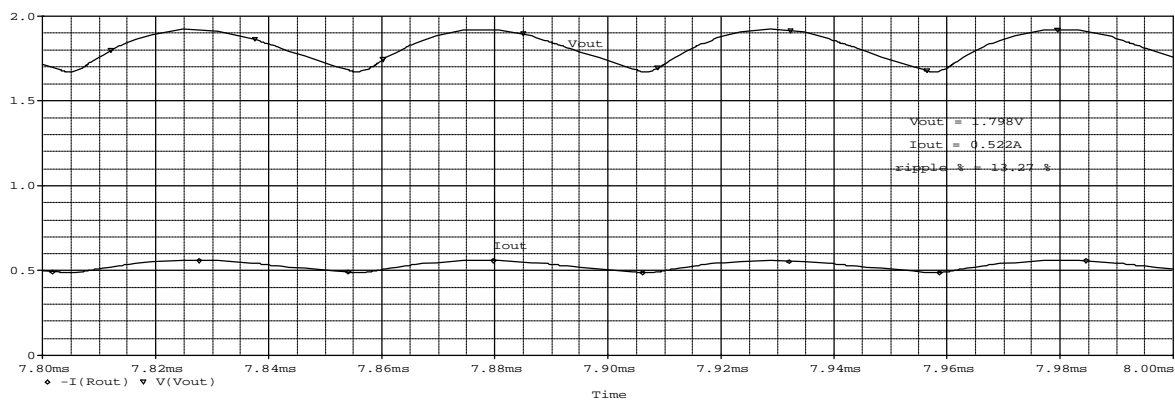


Fig.(14) : The waveform patterns in discontinuous conduction mode for V_{out} , I_{out} in case of the battery is on, $D<0.5$.

As seen in Fig. (13) and (14) the output voltage drops 6.5V for 0.52A at $D < 0.5$ (0.1) but the output voltage rises 3V at $D > 0.5$ (0.7).

For all three modes figures, the simulation results for PV pspice model match closely the results obtained from the battery.

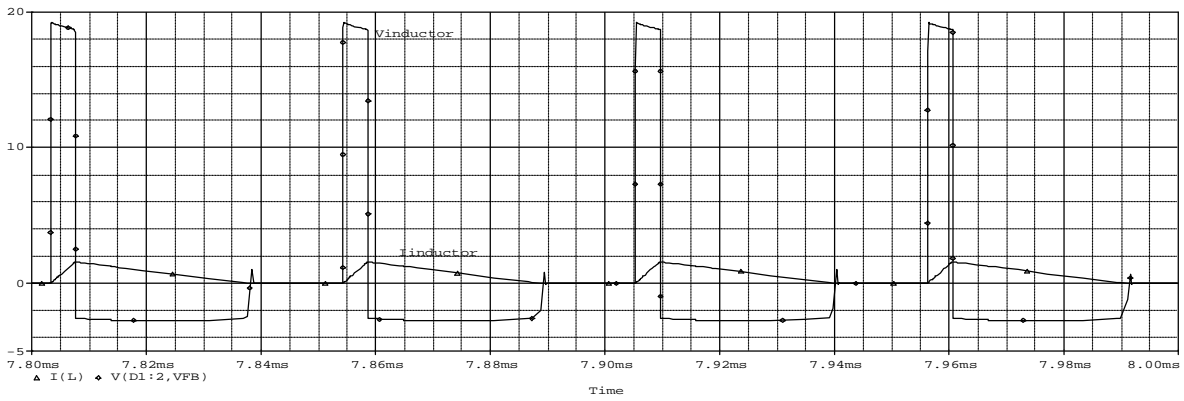


Fig.(15) : The waveform patterns in discontinuous conduction mode for $V_{inductor}$, $I_{inductor}$ in case of PV panel is on, $D < 0.5$.

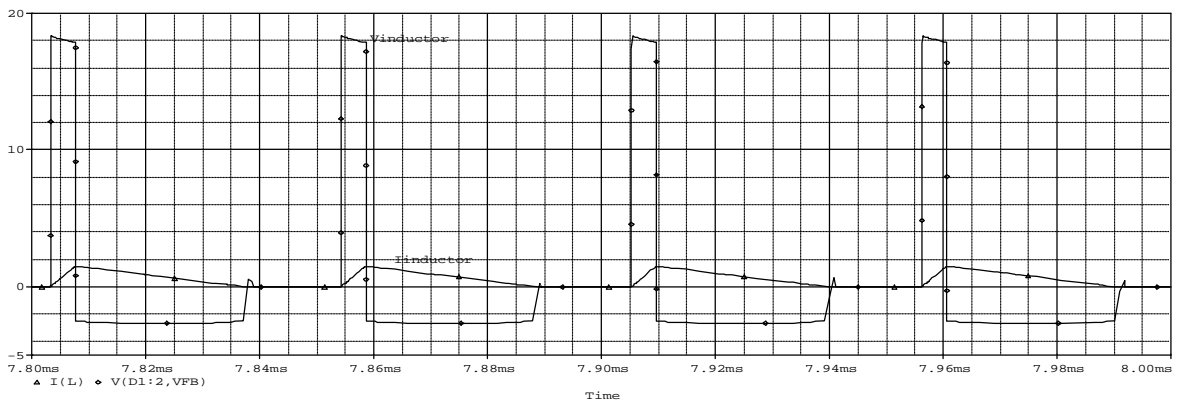


Fig.(16) : The waveform patterns in discontinuous conduction mode for $V_{inductor}$, $I_{inductor}$ in case of the battery is on, $D < 0.5$.

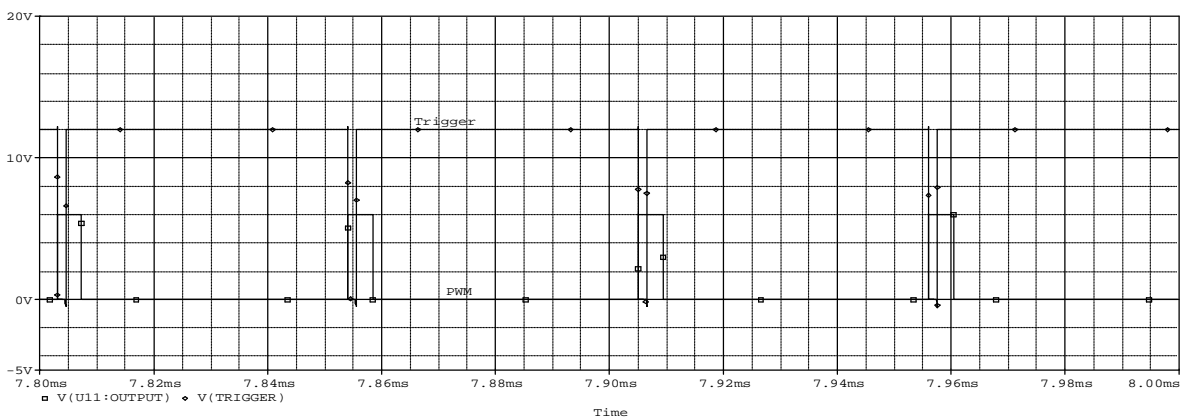


Fig.(17) : The waveform patterns in discontinuous conduction mode for $V_{trigger}$, V_{pwm} in case of PV panel is on, $D < 0.5$.

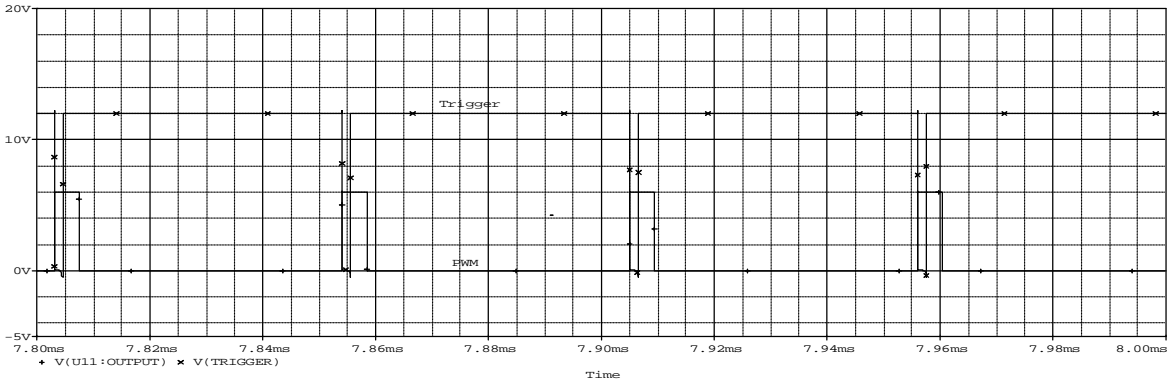


Fig.(18) : The waveform patterns in discontinuous conduction mode for $V_{triggers}$, V_{pwm} in case of the battery is on, $D < 0.5$.

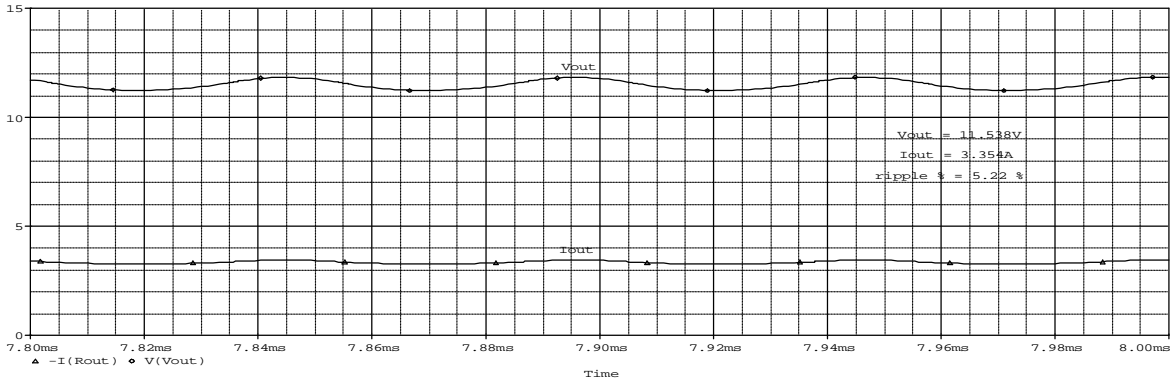


Fig.(19) : The waveform patterns in continuous conduction mode for V_{out} , I_{out} in case of PV panel is on, $D > 0.5$.

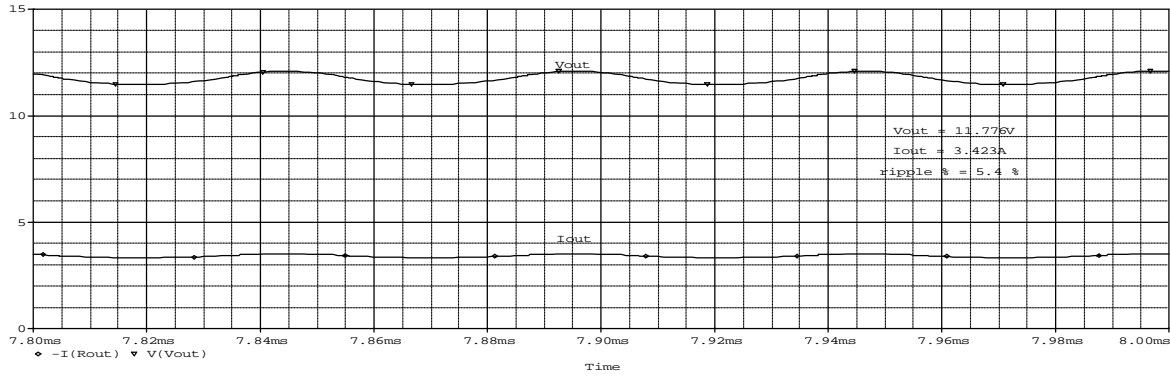


Fig.(20) : The waveform patterns in continuous conduction mode for V_{out} , I_{out} in case of the battery is on, $D > 0.5$.

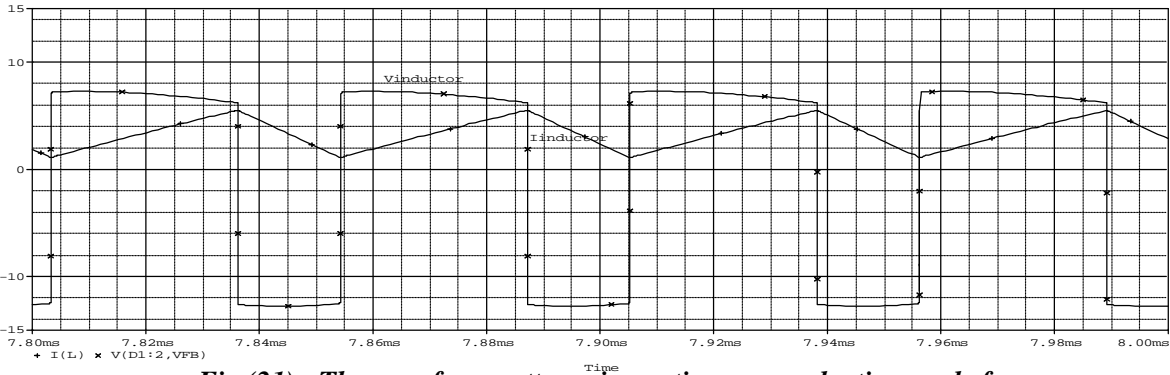


Fig.(21) : The waveform patterns in continuous conduction mode for $V_{inductors}$, $I_{inductor}$ in case of PV panel is on, $D > 0.5$.

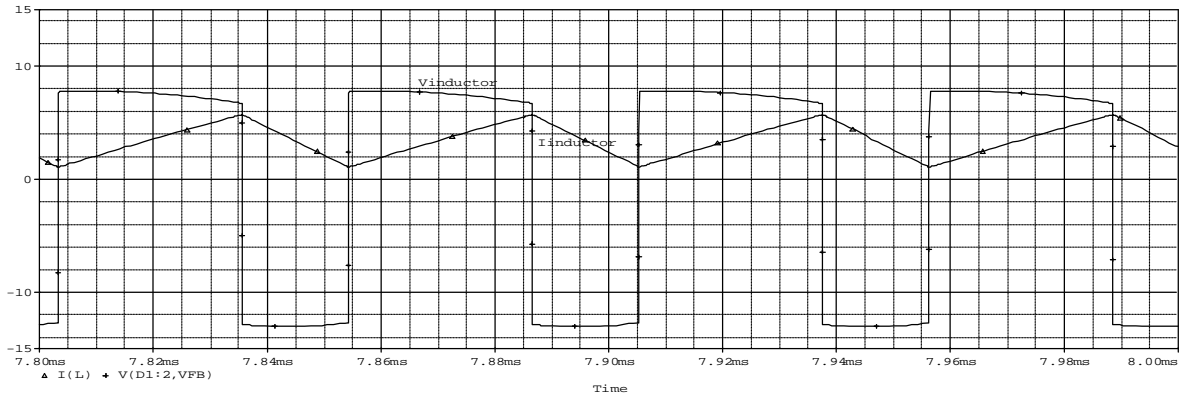


Fig.(22) : The waveform patterns in continuous conduction mode for $V_{inductor}$, $I_{inductor}$ in case of the battery is on, $D > 0.5$.

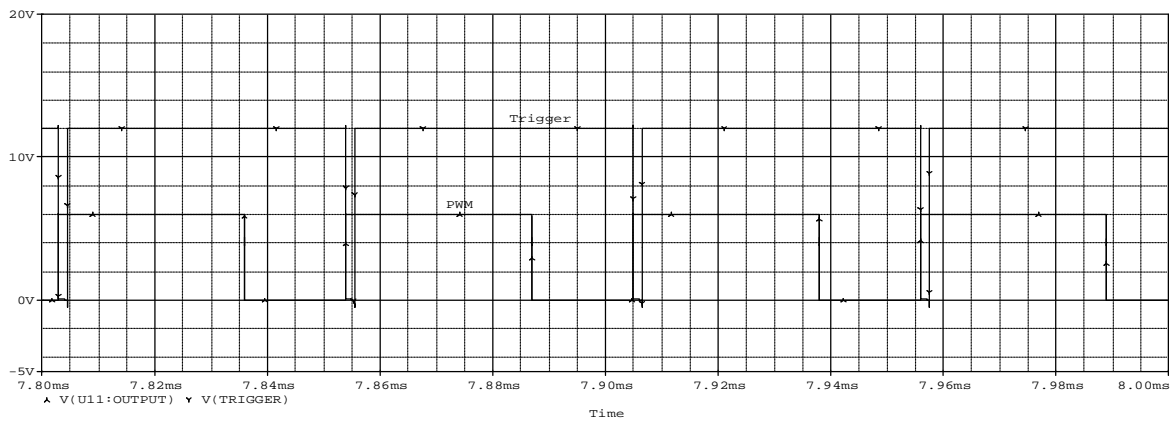


Fig.(23): The waveform patterns in continuous conduction mode for $V_{trigger}$, V_{pwm} in case of PV panel is on, $D > 0.5$.

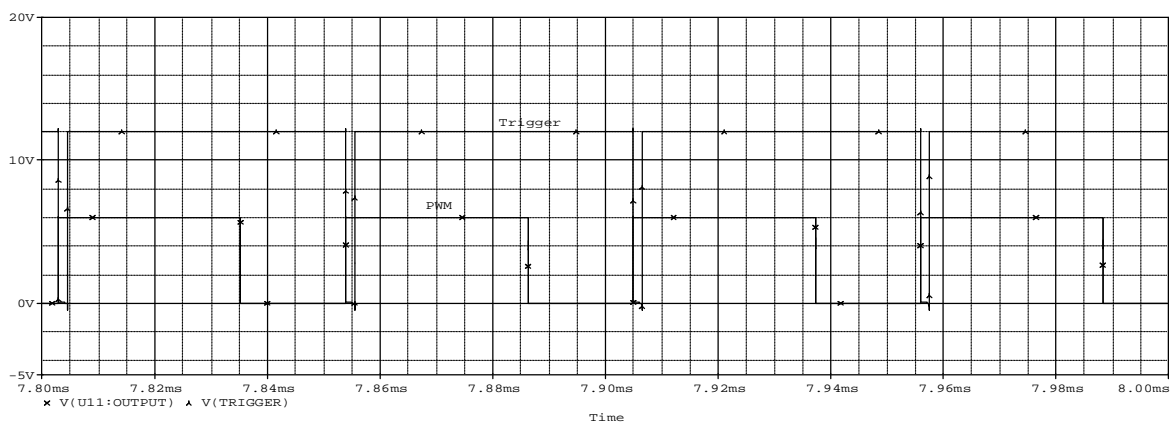


Fig.(24) : The waveform patterns in continuous conduction mode for $V_{trigger}$, V_{pwm} in case of the battery is on, $D > 0.5$.

Conclusion

The two input dc-dc buck converter has been proposed to combine and exploit several clean energy sources. As a result, the following points are clarified:

1. This converter was simulated in pspice to improve the validity of the PV panel model. This is achieved by comparing the results of the converter with a dc battery to that with the PV panel model. The converter with two sources gave us comparable results with a good agreement between them.
2. The PV model can be used for training personnel in the basic operation of solar energy systems.

References

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- [5] Everett Rogers " *Understanding boost power stages in switch mode supplies*", application report, Texas Instruments, 1999.

الخلاصة

هذا البحث يتعامل مع تصميم وتحليل مغير ذو مدخلين. المدخل الاول هو لوح شمسي والاخر هو البطارية. تم تمثيل اللوح الشمسي باستخدام الدائرة المكافئة المطورة في برنامج orcad pspice استخدام الدائرة المكافئة جعلت من الممكن ان نفحص خواص اللوح الشمسي. قدم البحث لنتائج تحليل المغير ولاساليب العمل الثلاثة *boundary, continuous and discontinuous*. نتائج تحليل المغير مع اللوح الشمسي اعطت تطابق جيد لتلك المقاسة مع البطارية.